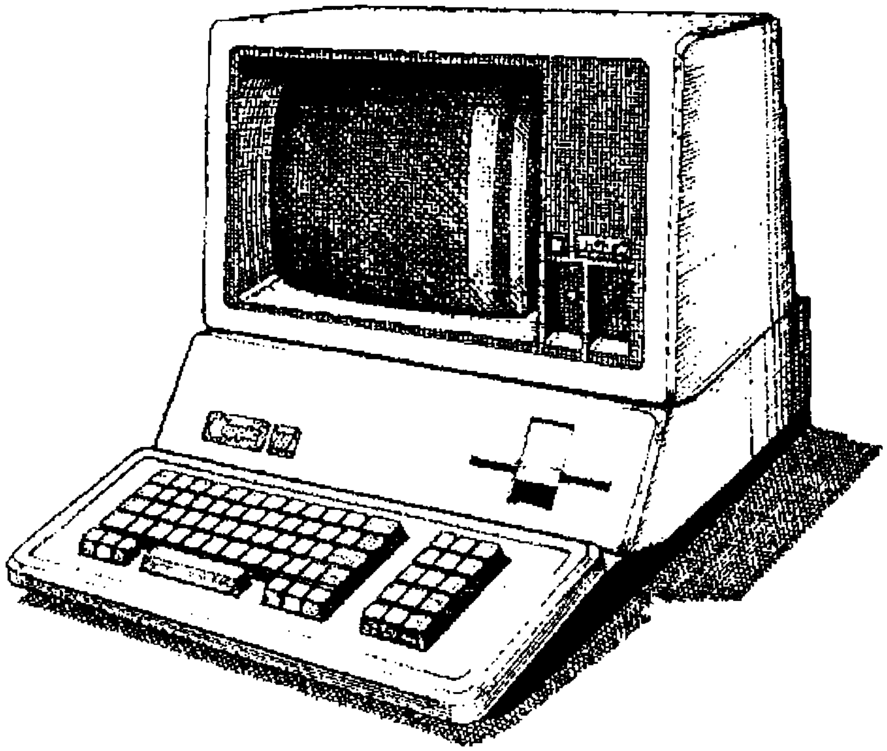
Apple /// Computer Information

Apple /// Service Reference Manual



Section I of II • Theory of Operation

Chapter 5 • System Clocks & Timing

Written by Apple Computer • 1982

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SYSTEM CLOCKS & TIMING

MAIN CLOCK (C14M)

The Apple /// has as its master clock a 14 megahertz crystal controlled oscillator. The active components of the clock circuitry are Q10, Q11, and Y1. The exact frequency of the oscillator is 14.318 MHz. The slight increase over 14 MHz is compensated for in other logic. Device B13 provides buffering and power amplification to drive all the other loads on the C14M and C14M* lines.

FREQUENCY DIVIDER

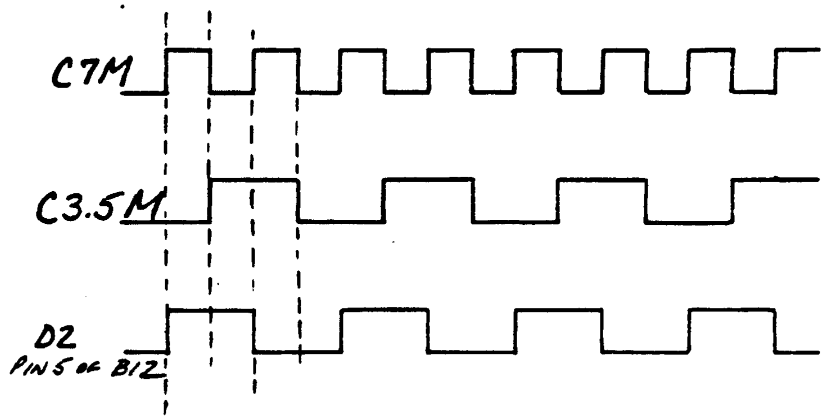
The next circuit in the system clock section is the frequency divider formed by device B12 and B13. This develops both the C7M* and the C3.5M*.

The C7M signal is developed by clocking the Q* output into the data input of a D-type latch. This results in a divide-by-two function of the clock frequency.

The C3.5M clock is developed in the same manner. However, the data input to the latch is an Exclusive-Or function of C7M and C3.5M at B13. This accomplishes two functions:

- o it divides the C14M clock by 4, and
- o it gives a definite phase relationship of C7M to C3.5M clocks.

Looking at the timing diagram below we see that the D2 input of B12 is high if either the C7M or the C3.5 clock is high but not when both are high. This function is effectively at 3.5 MHz which toggles on the positive edge of the 7MHz clock. The true C3.5M signal toggles on the negative edge of the C7M clock.



"Q" TIMING

The Q clocks are a series of 2 MHz clocks which are out of phase with one another by one clock time (refer to the Apple /// Timing diagrams). The rest of the system timing depends on the states of the "Q" outputs. They provide the basis

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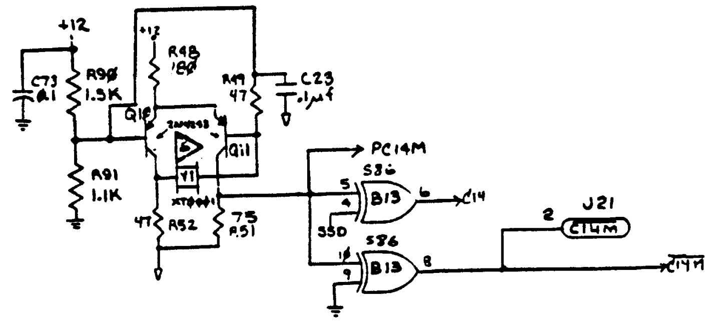
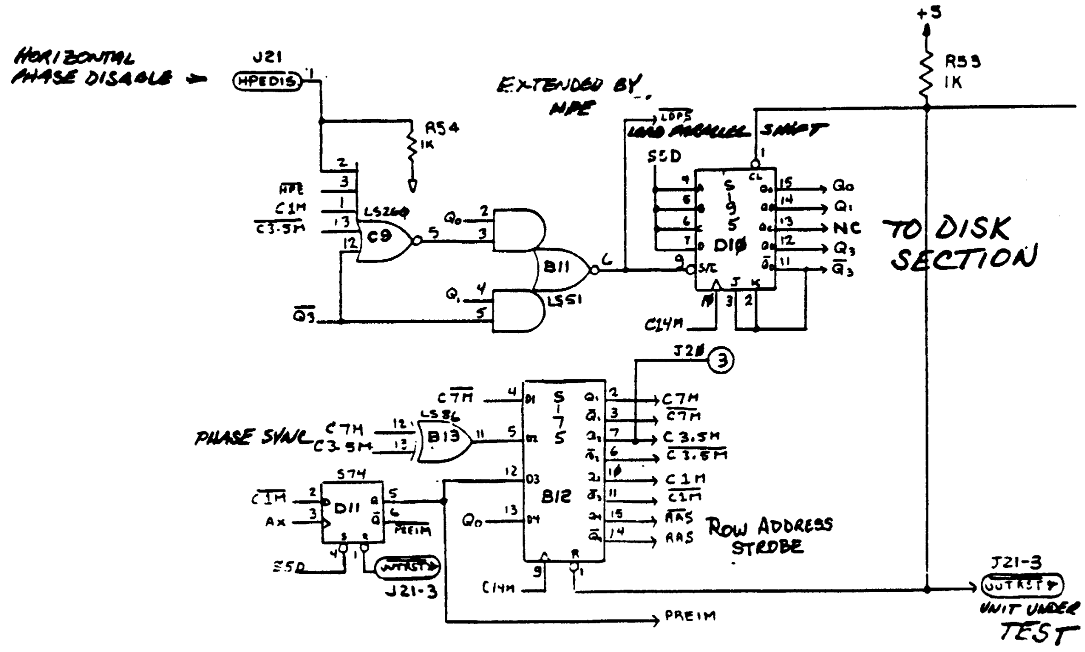
MAIN CLOCK - 14MHz



FREQUENCY DIVIDER.



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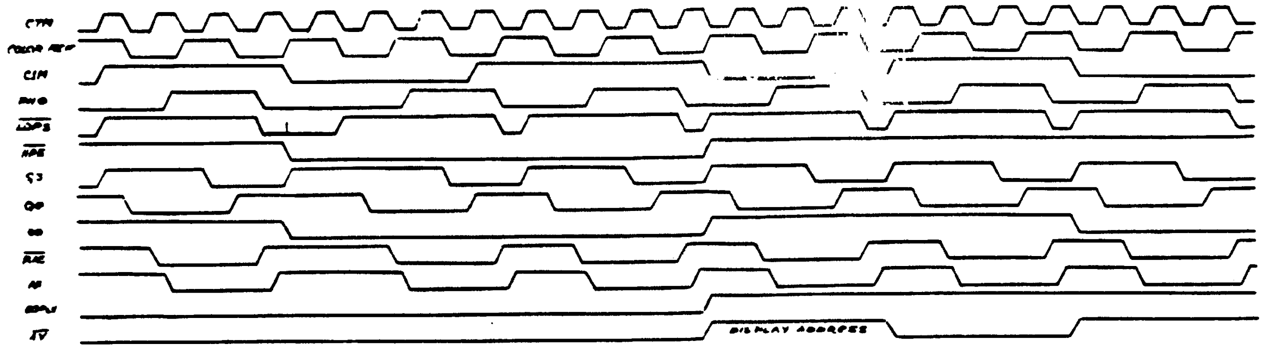
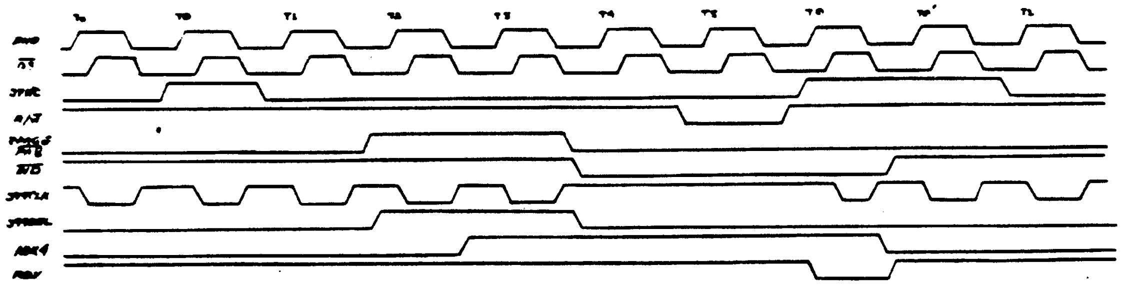
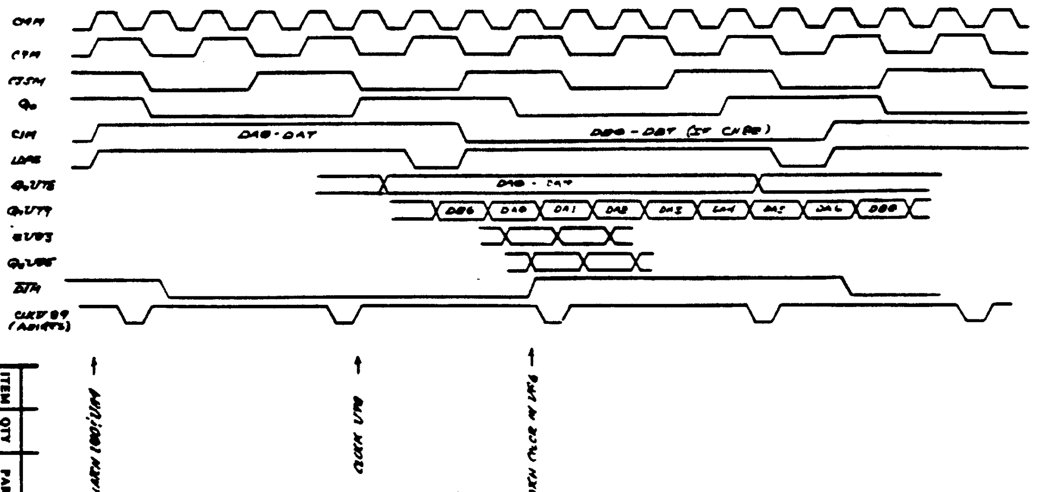


EXTRA NPE CYCLE & DISPLAY TIMING



INDIRECT ADDRESS TIMING



VIDEO SIGNALS

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

NEXT ASSY	
FINISH	
MATERIAL	

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± .XX ± .XXX ±
ANGLES ±
FRACTIONS ±
DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS

ITEM	QTY	PART NUMBER	DESCRIPTION

DRAWN BY	DATE
CHECKED BY	DATE
APPROVED BY	DATE
RELEASED BY	DATE

apple computer

TITLE

SIZE C

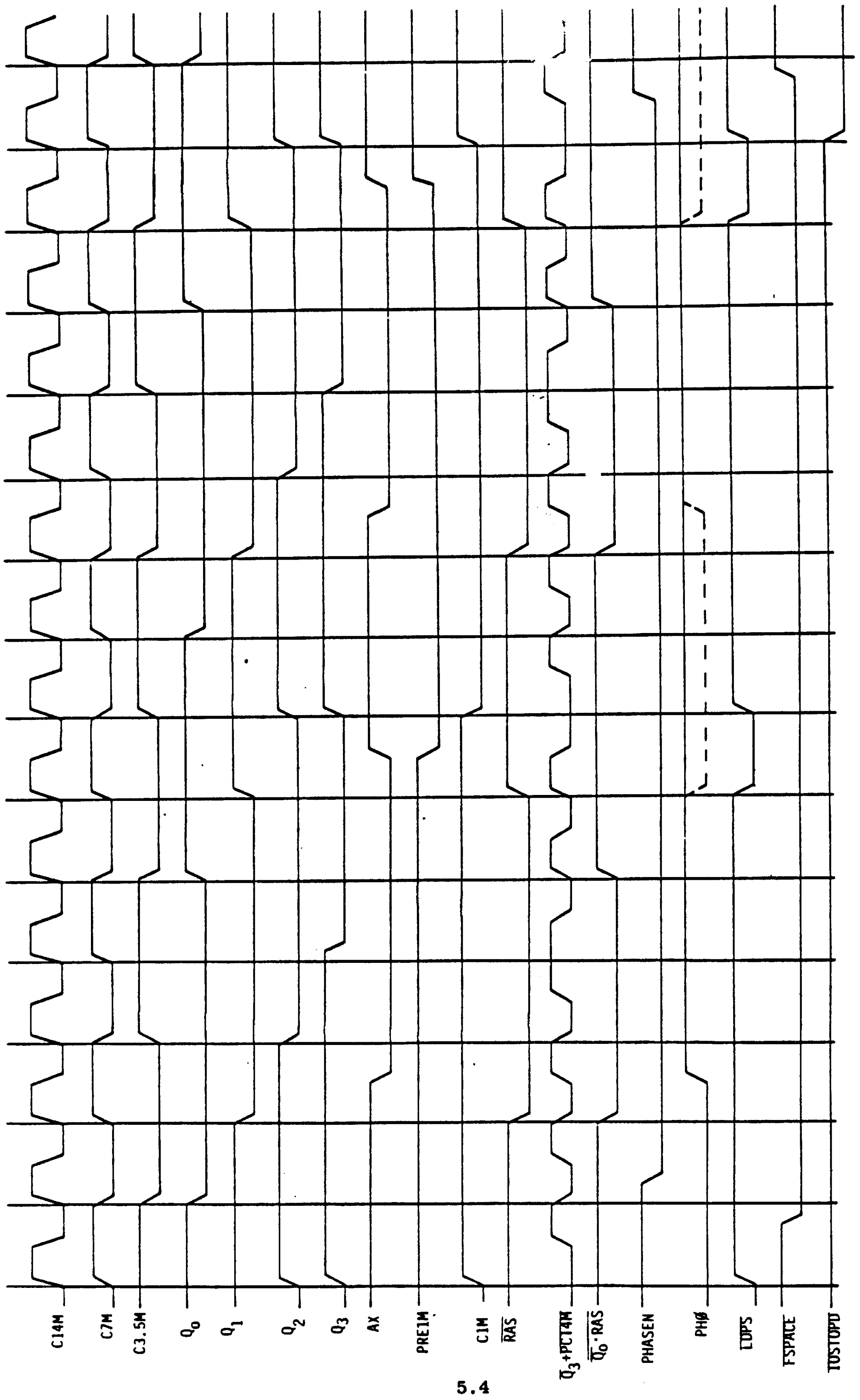
SCALE

DRAWING NUMBER

SHEET

A /// SYSTEM TIMING

5.3



APPLE III TIMING

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for processor and RAM address timing.

The Q clocks are initialized with each Load Parallel to Serial pulse (LDPS), which changes the mode of the LS195 (D10) from a shift register to a parallel loaded register when low. At each load, all of the bits are set high. When LDPS* returns high the next clock will shift the zero of Q3* across the register. This means that Q0 will stay high for one clock cycle. Q1 will stay high for 2 clocks, etc. When the Q3* goes high at the forth clock edge after LDPS the JK input will now see a "1". Subsequent clocks will start shifting that one across the register. When Q1 goes high again, LDPS* will be enabled low and another load will be accomplished at the next clock edge. The waveforms are assymmetrical. Each of Q0-Q2 are up for three clocks and down for four. Q3 is up for four and down for three.

This type of cycling will continue for 128 cycles. Then the Horizontal Phase Disable (HPE*) "freeze" will occur.

HPE* FREEZE

The HPE* signal will cause the Q states to extend their next cycle by two clock times. The purpose of the shift is to shift the phase of the color reference signals to the data in the video generator. A detailed discussion of this phenomenon is described in the video generator section. How this shift occurs is discussed below.

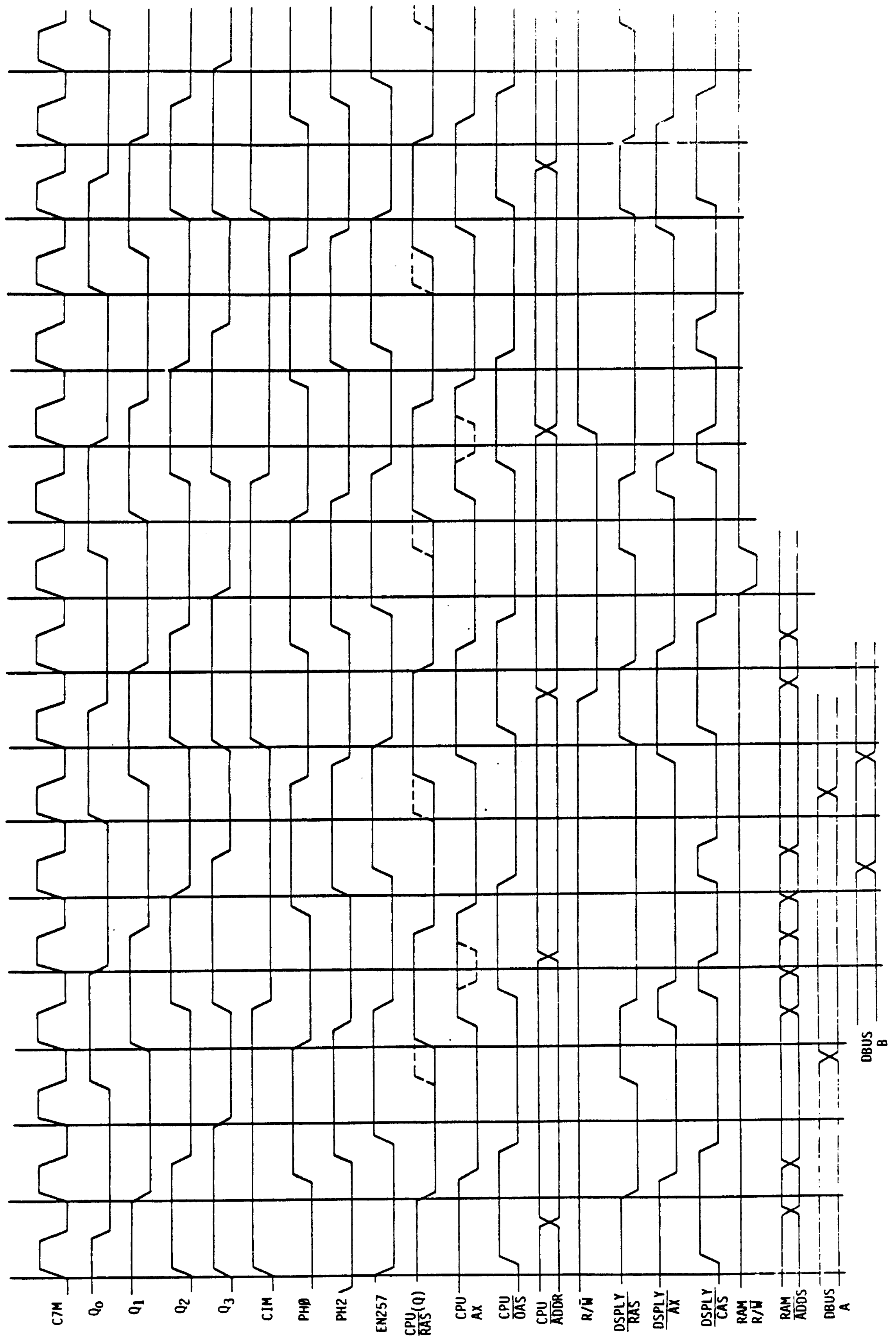
Looking at the gate array of C9 and B11 we see that since HPE* is normally high, the output of C9 is normally low. This de-gates the And inut shared with Q0, and allows LDPS to function as usual. But when HPE* goes low, which will always coincide with C14M going low, the And gate shared with Q0 will become enabled and cause the extension of the LDPS* for two extra clock cycles. This state will exist until C3.5M returns high and relieves LDPS*. The next clock will change the state of Q0 and that will not be able to "disrupt" the clocks until the next HPE pulse.

AX, PRE1M, & C1M

The AX, RAM address (the signal used to select which addressing source [row or column] is presented to the RAMs: see RAM Address Logic) is another 2 Mhz signal which lags Q1 by one half clock cycles. It is developed at A11 pin 9.

PRE1M can toggle at each positive edge of AX, if the data input to the latch is at the opposite state. Looking at D11 (C1M*) we will be able to see just that. If PRE1M has just toggled low, one half clock cycle later C1M* will toggle high which forms the data input to the PRE1M Flip-Flop. But remember, the clock to the flip-flop is AX, a 2 MHz signal. D11 pin 5 acts much like B12 pin 2 in that the data is always opposite to the "Q" output of the latch at the time of the clock edge, therefore we have a "clock divided by 2" function, of a 1 MHZ output.

RAS (Row Address Strobe)


C7M
Q0
Q1
Q2
Q3
C1M
PHØ
PH2
EN257
CPU RAS(Q)
CPU AX
CPU OAS
CPU ADDR
R/W
DSPLY RAS
DSPLY AX
DSPLY CAS
RAM R/W
RAM ADDS
DBUS A
DBUS B

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The RAS signal is Q0 delayed by one clock and inverted. This is acccomplished at D10 pin.15 & 14. (Note: the inversion is done by calling the "Q" output the active low signal RAS*, clever huh?) RAS is used in the RAM address logic to develop the "row select" signals for the RAMs.

VIDEO HORIZONTAL & VERTICAL STATE COUNTERS

This circuit is made up of four 4-bit binary counters, (F10, F11, G11, G12), which develop the essential signals for partitioning the screen and addressing the RAM for all the video data.

Basically, there are two sections of the circuit:

1 - horizontal postion counter

2- vertical position counter

These two counters form the X and Y coordinates of each addressable byte on the screen. Each byte contains 7 bits or dots in 40 character modes.

From the various discussions about the Apple ///, we have learned that in the 40 character mode there are 280 dots across the horizontal line that can be defined, and 192 of these horizontal line (280 X 192). In the Apple /// modes there are 560 dots in the horizontal line, however, there are still only 192 horizontal lines (560 X 192).

The Video Counter works identically in either of these modes. It provides the resolution of 40 by 192 matrix. Each one of the 40 horizontal positions defines either 7 or 14 dots (40 or 80 character modes, respectively). These dots are actually bits of data bytes in memory that are parallel loadedd into a shift register and shifted out serially to the video monitor. In the 40 character modes the system loads the shift register at a 1 MHz rate and shifts at a 7 MHz rate. In the 80 character modes it loads at a 2 MHz rate and shifts at a 14 Mhz rate. It is interesting to note that in either mode the state counter increments at a 1 Mhz rate.

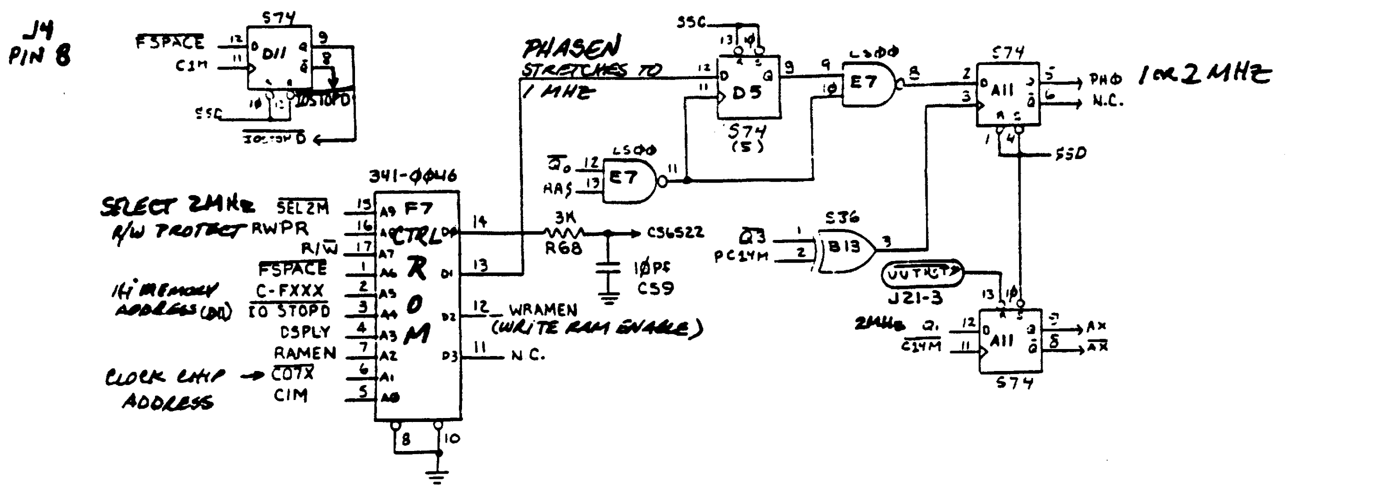
The system provides two complete accesses for the video output per increment of the state counter, but in the 40 character modes one of these are masked out.

HORIZONTAL SECTION

The Horizontal section of the state counter uses 7 of the counter stages and develops the H0 through H5 and the HPE* signals. The remaining 9 stages of the counter develop the Vertical states VA, VB, VC, and V0 through V5.

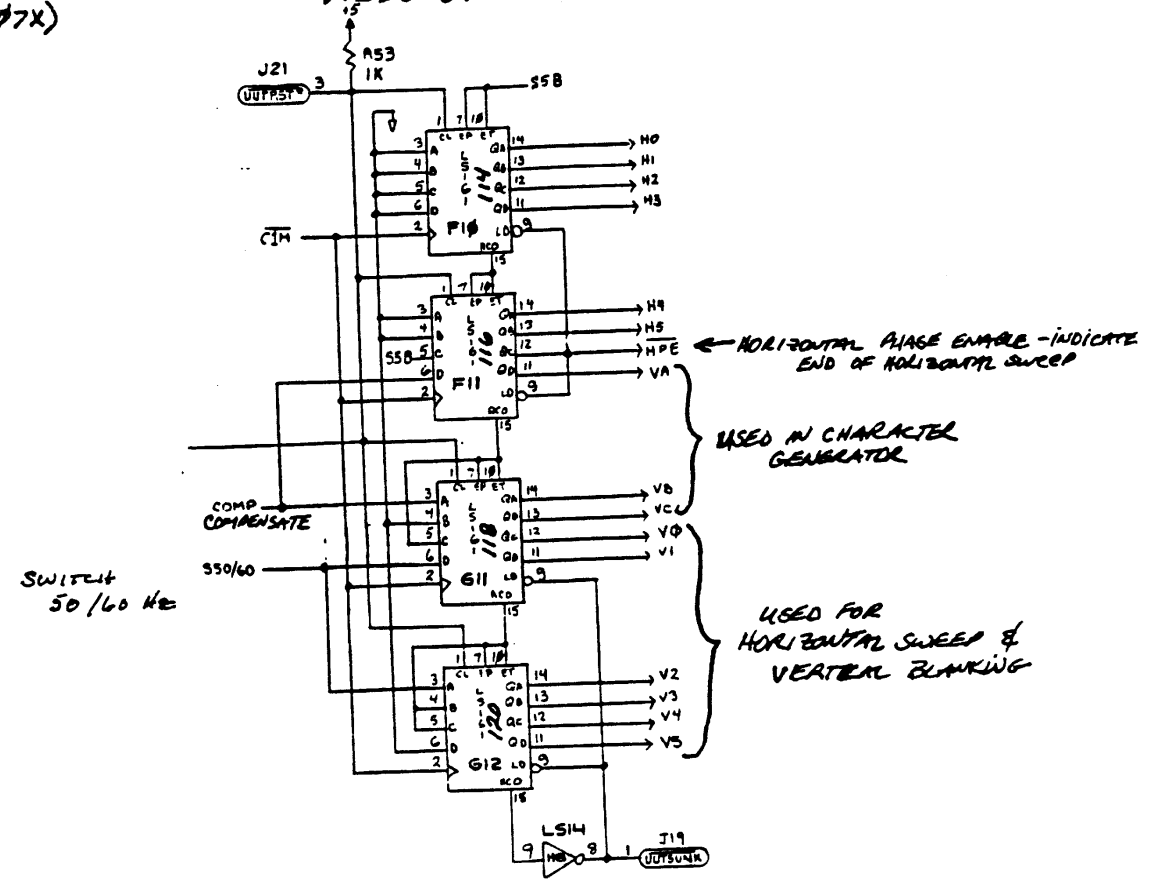
The Horizontal section provides the capability of a 128 state counter, however, it only provides 65 states. This is due to the action of the most significant stage, HPE*. The counter actually counts from 64 to 128 then resets to count 64. Simply, HPE* starts high and when the counter increments HPE* low after 64 counts it is then reset to state 64 after the next clock input, this yields

1 TO 2 MHz GEARSHIFT



FSPACE – RESULTS WHEN YOU ADDRESS THE VIA'S, THE ACIA, OR THE INTERNAL CLOCK (C07X)

VIDEO STATE COUNTER


+5
R53 1K
J21
SSB
F10
H0
H1
H2
H3
C1M
F11
H4
H5
HPE
HORIZONTAL PHASE ENABLE – INDICATE END OF HORIZONTAL SWEEP
VA
USED IN CHARACTER GENERATOR
COMP COMPENSATE
G11
VB
VC
VΦ
V1
SWITCH 50/60 Hz
S50/60
USED FOR HORIZONTAL SWEEP & VERTICAL BLANKING
G12
V2
V3
V4
V5
LS14
J19

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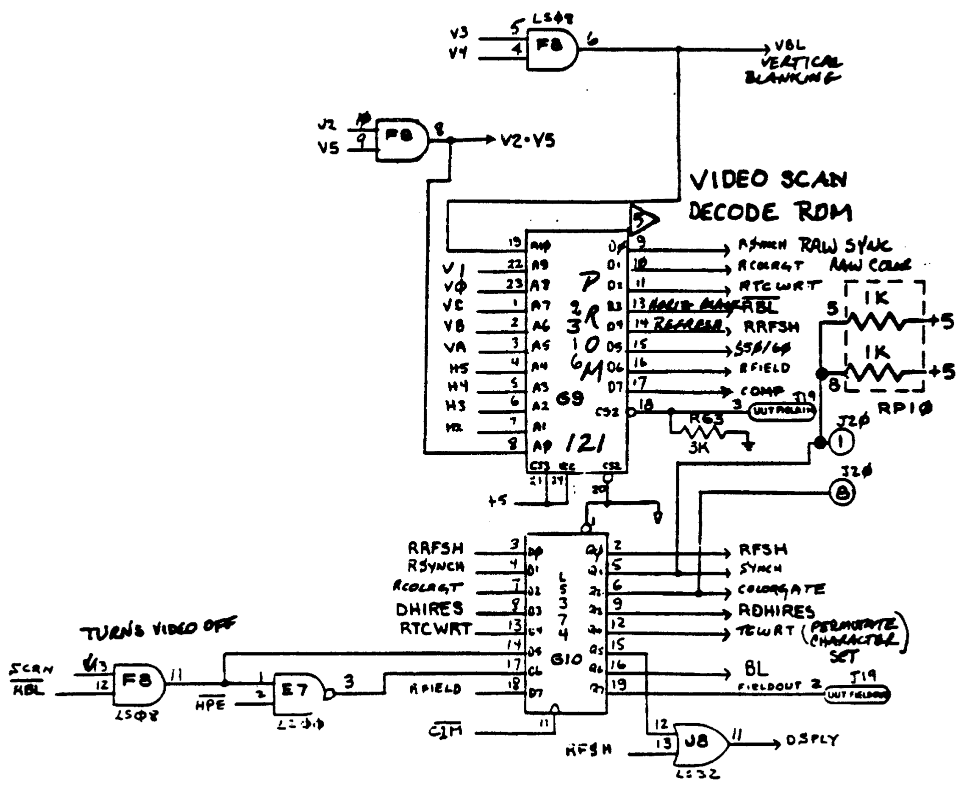

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65 states all together.

Looking at F11 we see that the HPE* output is connected to the "load" input of F10 and F11. At the next clock input these two devices will be loaded with the state determined by what is on the data inputs. All inputs except pin 5 of F11 are tied low (disregard the input to pin 6 of F11 at this time). This binary state equals 64. So rather than starting back at "zero" the counter jumps to 64.

For real time considerations of the monitor, it takes 25 states or 25 microseconds for the sweep to return from the right hand side to the left side. So the system ignores the first 25 states and blanks the video output and the returning trace is not shown. The boolean expression for the horizontal blanking would be expressed:

(H4* and H5*) or (H4 and H3*)

This logical function is done within the G9 Control ROM. Refer to page 10 of 10 of the schematic diagram.

In summary, the horizontal counter provides the address necessary for the display. It divides the horizontal line into forty (40) sections, and yields the timing for horizontal blanking. The HPE* signal is used to momentarily "freeze" some of the system timing.

VERTICAL SECTION

The Vertical State Counter provides the Y-axis of the display matrix. The nine stages, if left alone to count, would provide 512 states. As in the horizontal counter, it is preset to count higher than zero eadch time it reaches the "terminal count". Also, some of the states are used to blank the video while the trace returns from the bottom of the screen to the top (VBL).

The vertical counter effectively counts the number of HPE*'s that have occurred, or simply, the number of horizontal lines that have been generated in this scan.

At this time the counter is reset to count 250. Look at the timing diagram of the vertical counter. One can see that all vertical signals would normally go low, but instead the counter is loaded with the data inputs. VA will not be affected by the teminal count/load and will continue as discussed before. VB will be loaded to the present state of "comp" (or VA) which is high. VC and V5 will be loaded to a low and the rest of the bit states wil be loaded to "1". This will decode to decimal 250.

Six counts later VA through V4 will toggle low and V5 will toggle high. This is the point where the logic assumes to be at scan line "zero". It will now take 256 counts to reach the terminal count sequence and start again. Using some math we see that the counter defines 262 states (256+6 = 262).

Vertical blanking takes 70 of the 262 states developed by the counter. The boolean expresssion for the vertical blanking signal would be:

(V3 and V4)

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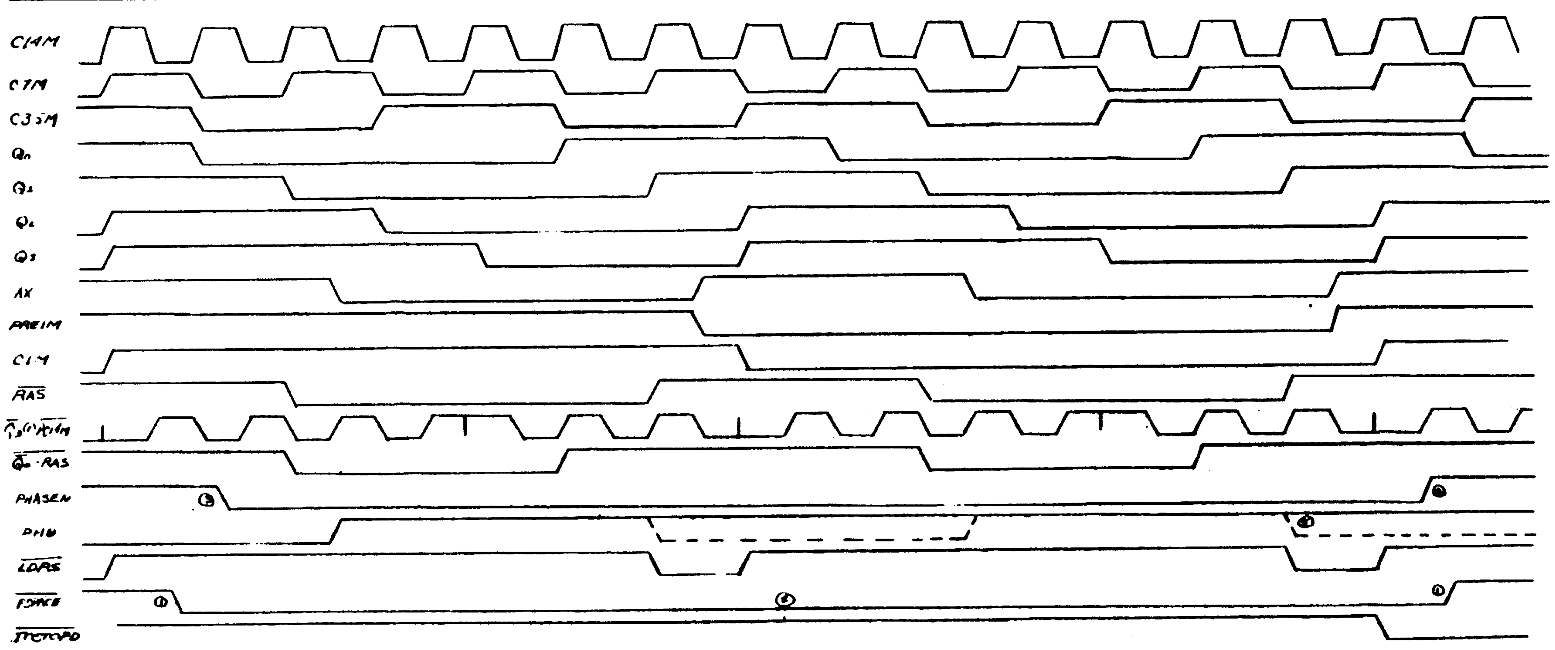
This signal is developed at F8 pin 6 and is used in the system to indicate that a complete scan of the current display page has occurred. It is also an input to the Control Rom, G9, and therefore is a modifier to its outputs.

We were looking for the majic number of 192. Well, if you´ve been keeping track, it´s simply the difference of 272-70.

4 3 2 1

REV.	ZONE	ECO #	REVISION

NOTE: UNLESS OTHERWISE SPECIFIED



D
C
5.12
B
A

① ADDRESS TIME FROM PHØ
② FSPACE MAINTAINED BY PHØ STRETCH
③ PHASEN CASE: 3.58M · $\overline{IOSTOPD}$ · FSPACE
④ PHASEN GOES HIGH DUE TO $\overline{IOSTOPD}$
⑤ PHØ HELD HIGH ANOTHER CYCLE TO SYNCH 6522'S TO C1M

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

APPLE /// SYSTEM TIMING

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ___
.XX ± ___
.XXX ± ___
ANGLES XX.X ± ___
FRACTIONS ± ___
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS

DRAWN BY	DATE
CHECKED BY	DATE
APPROVED BY	DATE
RELEASED BY	DATE

MATERIAL:

NEXT ASSY | FINISH:

apple compu

TITLE
APPLE /// TIMI

SIZE B | DRAWING NUMB

SCALE: | SHEET

4 3 2 1