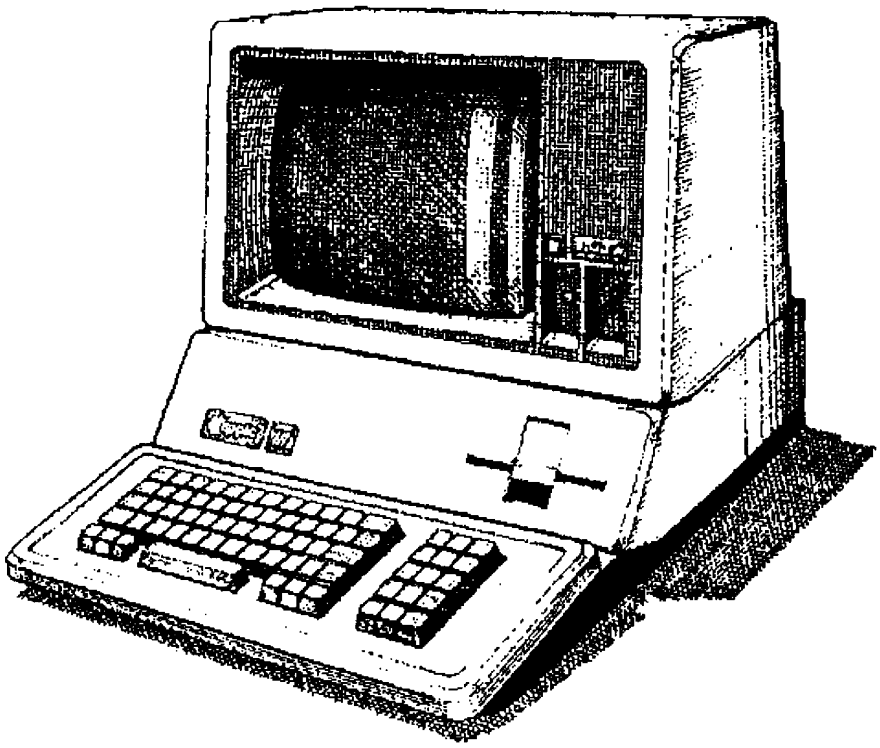
Apple /// Computer Information

Apple /// Service Reference Manual



Section I of II • Theory of Operation

Chapter 10 • Apple][Emulation

Written by Apple Computer • 1982

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APPLE II EMULATION RESTRICTIONS

- NO LANGUAGE CARD
- NO ROM CARD
- PADDLES ARE DIFFERENT
- ENTER WITH SOFTWARE BUT ONLY RESET WILL EXIT

THE COLOR VIDEO CONNECTOR

Pin	Name	Description
1	SG	Shield Ground.
2	XRGB4	One of four GRB outputs. This (and pins 5, 9, and 10) is a TTL output with instantaneous color information. A linear weighted sum of these four signals will form a true 16-color RGB video signal
3	SYNCH	Composite synchronization signal with negative-going tips.
4	PDI	Not used.
5	XRGB1	See pin 2.
6	GND	Power and signal ground.
7	-5V	-5 volt power supply. A device may draw up to 200 ma through this pin.
8	+12V	+12 volt power supply. A device may draw up to 500 ma through this pin.
9	XRGB2	See pin 2.
10	XRGB8	See pin 2.
11	BWVID	Black and white composite video. This is an NTSC composite video signal with negative-going synch tips, 1 volt peak-to peak into a 75 ohm load. Color information is encoded as a linear grey scale.
12	NTSC	Color composite video. This is an NTSC-compatible video signal with negative-going sych tips, 1 volt peak-to-peak into a 75 ohm load.
13	GND	Power and signal ground.
14	-12V	-12 volt power supply. A device may draw up to 200 ma through this pin.
15	+5V	+5 volt supply. A device may draw up to 1 amp through this pin.

This connector supplies 7 different video signals and 4 power supply voltages. Through this connector you can hook up the Apple to any NTSC color or black and white video monitor. With an additional circuit you can hook up the Apple to a studio-quality RGB color monitor.

All power supply current ratings assume that no peripheral cards are installed in the system. If there are cards in the system, be sure to account for the current drawn by those cards.

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THE HIGH-RESOLUTION GRAPHICS (HI-RES) MODE

The Apple][emulation mode high resolution graphics are identical to the Apple][except some combinations of colors on the right edge of the screen will cause the left edge pixels to blink. This is normal though distracting.

THE SPEAKER

The speaker function is identical to the Apple][with the following additional features.

A reference to location 49216 (or the equivalent addresses -16336 or hexadecimal $C040) will cause a 0.1 second 1 KHz tone to be produced which is similar to the sound the AUTOSTART monitor makes when the BELL character is sent to the screen. The advantage to this is 0.1 seconds of cpu time is returned to the user since only 1 microsecond is required to start the BELL sound.

The AUDIO connector at the back of the Apple /// provides the same signal as the speaker. When you insert a miniature phone-tip plug into this jack, the Apple's internal speaker is silenced; if there is an amplifier or other device properly connected to the plug, then that device will receive all audio signals generated by the Apple. The signal is a 0.5 volt peak-to-peak audio signal on its tip and signal ground on its ring.

THE CASSETTE INTERFACE

The cassette interface is completely eliminated on the Apple ///. References to the cassette output port at 49184 (or the equivalent -16352 of hexadecimal $C020) will cause pin 39 of the I/O slots to go low for a microsecond. This is for use by Apple /// native mode peripherals to deselect to $C800 ROM address space.

Reading the cassette input port at 49248 or the equivalents -16288 or hexadecimal $C060 will read joystick switch 0 into bit 7.

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Table 10: Input / Output Special Locations

Function	Address: Decimal		Hex	Read/Write
Speaker	49200	-16336	$C030	R/W
Beep	49216	-16320	$C040	R/W
Deselect $C800 for Apple /// peripherals (pin 39 in slots)	49184	-16352	$C020	R/W
Joystick switch 0	49248	-16288	$C060	R(bit 7)
Joystick switch 1	49249	-16287	$C061	R(bit 7)
Joystick switch 2	49250	-16286	$C062	R(bit 7)
Joystick switch 3	49251	-16285	$C063	R(bit 7)
$\overline{\text{A/D Select 0}}$	49240	-16296	$C058	R/W
A/D select 0	49241	-16295	$C059	R/W
$\overline{\text{A/D Select 1}}$	49246	-16290	$C05E	R/W
A/D Select 1	49247	-16289	$C05F	R/W
$\overline{\text{A/D Select 2}}$	49242	-16294	$C05A	R/W
A/D Select 2	49243	-16293	$C05B	R/W
A/D Ramp charge	49244	-16292	$C05C	R/W
A/D Start timeout	49245	-16291	$C05D	R/W
$\overline{\text{A/D Timeout}}$	49254	-16282	$C066	R(bit 7)
Clock millisecond counter ($N0)	49264	-16272	$C070	R(bits 7-4)

Table 9: A/D Selection

A/D 2	A/D 1	A/D 0	Input
0	0	0	Ground
0	0	1	Joystick, Port B, X axis
0	1	0	Joystick, Port B, Y axis
0	1	1	Joystick, Port A, X axis
1	0	0	Joystick, Port A, Y axis
1	0	1	Clock Battery
1	1	0	No connection
1	1	1	Reference Voltage

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ANALOG INPUTS

The system has two joystick ports with provisions for two A/D inputs each. Joystick Port A reads A/D inputs 0 and 2 while Port B reads inputs 1 and 3 as defined in BASIC and the monitor subroutine PREAD.

To read the A/D inputs, the software must select the desired input and charge the ramp capacitor for at least 500 microseconds. Then the ramp is started and the time measured until the A/D timeout goes low. The discharge time is proportional to the input voltage.

STROBE OUTPUT

The strobe output ($C040) has been replaced by a 0.1 second 1 KHz tone from the speaker.

AUTOSTART ROM / MONITOR ROM

The Apple][emulation only comes with a modified version of the Autostart ROM. This is in write protected RAM which is loaded when the Apple][emulation disk is booted.

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THE SYSTEM MONITOR

SAVING A RANGE OF MEMORY ON THE TAPE

Since there is no cassette port on the Apple /// the W (for WRITE) command has no effect. The code in the Emulation mode Autostart Monitor contains an RTS instruction followed by NOP instructions, followed by BRK instructions. This fills the space occupied by the WRITE subroutine (locations $FECD-$FEF4).

READING A RANGE FROM TAPE

Again, since there is no cassette port the R (READ) command has no effect. The READ subroutine contains an RTS followed by NOP instructions, followed by BRK instructions (locations $FEFD-$FF2C).

SOME USEFUL MONITOR SUBROUTINES

$FB1E PREAD READ A JOYSTICK AXIS

PREAD will return a number which represents the position of a joystick axis. You should pass the number of the joystick axis (0 to 3) in the X register. If this number is greater than 3, port A, Y axis is read. PREAD returns a number from $00 to $FF in the Y register. The accumulator is scrambled.

Joystick	Reference #
Port A, X axis	0
Port B, X axis	1
Port A, Y axis	2
Port B, Y axis	3

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Page Three Monitor Locations

Address: Decimal	Hex	Use:
1008	$3F0	Holds the address of the subroutine which handles machine language "BRK" requests (normally $FA59).
1009	$3F1	
1010	$3F2	Soft Entry Vector. These two locations contain the address of the reentry point for whatever language is in use. Normally contains $E003.
1011	$3F3	
1012	$3F4	Power-up byte. Normally contains $45.
1013	$3F5	Holds a "JuMP" instruction to the subroutine which handles Applesoft]["&" commands. Normally $4C $58 $FF.
1014	$3F6	
1015	$3F7	
1016	$3F8	Holds a "JuMP" instruction to the subroutine which handles "USER" (CONTROL Y) commands.
1017	$3F9	
1018	$3FA	

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Built-In I/O Locatons

	$0	$1	$2	$3	$4	$5	$6	$7
$C000	Keyboard Port A Input							
$C008	Keyboard Port B Input							
$C010	Clear Keyboard Strobe							
$C020	Deselect all expansion I/O space (pin 39) for Apple /// cards							
$C030	Speaker Toggle (1us) pulse							
$C040	Speaker Beep (1 KHz for 0.1 second)							
$C050	gr	tx	nomix	mix	pri	sec	lores	hires
$C058	$\overline{\text{A/D 0}}$	A/D 0	$\overline{\text{A/D 2}}$	A/D 2	A/D CHG	A/D ST	$\overline{\text{A/D 1}}$	A/D 1
$C060	SW0	SW 1	SW 2	SW 3	$\overline{\text{IRQ 2}}$	$\overline{\text{IRQ 1}}$	$\overline{\text{A/D TM}}$	MUX1
$C070	Clock millisecond output (SN0)							
$C090-$C09F	Slot 1 Device Select (pin 41) goes low during C1M							
$C0A0-$C0AF	Slot 2 Device Select (pin 41) goes low during C1M							
$C0B0-$C0BF	Slot 3 Device Select (pin 41) goes low during C1M							
$C0C0-$C0CF	Slot 4 Device Select (pin 41) goes low during C1M							
$C0E0	$\overline{\text{Disk Stepper Motor Phase A}}$							
$C0E1	Disk Stepper Motor Phase A							
$C0E2	$\overline{\text{Disk Stepper Motor Phase B}}$							
$C0E3	Disk Stepper Motor Phase B							
$C0E4	$\overline{\text{Disk Stepper Motor Phase C}}$							
$C0E5	Disk Stepper Motor Phase C							
$C0E6	$\overline{\text{Disk Stepper Motor Phase D}}$							
$C0E7	Disk Stepper Motor Phase D							

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$C0E8 Disk motor off

$C0E9 Disk motor on

$C0EA Select Drive 1 (Built-in)

$C0EB Select Drive 2 (First external)

$C0EC Q6L

$C0ED Q6H

$C0EE Q7L

$C0EF Q7H

$C0F0 ACIA Receive/Transmit Data register

$C0F1 ACIA Status register

$C0F2 ACIA Command register

$C0F3 ACIA Control register

$C100-$C1FF Slot 1 I/O Select (Pin 1) goes low during C1M low

$C200-$C2FF Slot 2 I/O Select (Pin 1) goes low during C1M low

$C300-$C3FF Slot 3 I/O Select (Pin 1) goes low during C1M low

$C400-$C4FF Slot 4 I/O Select (Pin 1) goes low during C1M low

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PERIPHERAL BOARD I/O

The Apple /// implements only slots 1 through 4. Slot 6 is always a disk interface card and slots 5 and 7 emulate either a SERIAL or COMMUNICATIONS card. Slot 0 scratchpad RAM exists but no provision is made to put a LANGUAGE card or FIRMWARE card into the system. Thus the RAM is limited to 48K with a 12K ROM chosen at Boot time.

PERIPHERAL CARD I/O SPACE

Slot 6 device I/O space $C0E0-$C0EF contains the hardware for the disk interface. Slot 7 device I/O space $C0F0-$C0F3 contains the addresses for the onboard ACIA.

PERIPHERAL CARD ROM SPACE

Slot 5 and slot 7 contain code which is functionally equivalent to the COMMUNICATIONS or SERIAL card for the Apple][. They differ in that they use the built-in ACIA. For a more complete explanation see "SERIAL AND COMMUNICATONS CARD EMULATION ".

Slot 6 contains a copy of the Apple][16 sector Boot PROM.

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ROM MEMORY

The Applesoft, Integer Basic, and Autostart Monitor "ROMS" are actually write protected RAMs in the Apple ///. When the Emulation mode disk is booted it loads RAM memory with an image of each set of ROMs. Whichever language is selected when the Apple][disk is booted is loaded into the address space ($D000-$FFFF) and write protected.

RAM MEMORY

In Emulation mode there is always 48K of RAM. It is addressed $0000 to $BFFF. There is no provision for a slot 0 Language or Firmware card.

"USER 1" JUMPER

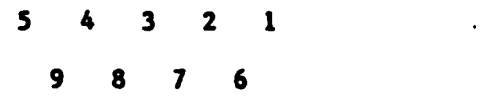
There is no "User 1" jumper in the Apple ///.

THE GAME I/O CONNECTOR

There is no 16 pin Game I/O connector in the Apple ///. However there are two 9 pin "D" - joystick connectors.

THE JOYSTICK PORTS

The Apple /// has to joystick ports (A and B). The A port will NOT operate a silentype printer in Emulation mode. The physical pinout is:



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PORT A PINOUT

Pin	Name	Description
1	SGND	Shield ground.
2	+5V	+5 volt power supply.
3	GND	Power and Signal Ground.
4	XO	Horizontal analog input, PDL (0) in BASIC.
5	SW1	Joystick switch 1, orange button.
6	+12V	+12 volt power supply.
7	GND	Power and signal Ground.
8	YO	Vertical analog input, PDL (2) in BASIC.
9	SW3	Joystick switch 3.

PORT B PINOUT

Pin	Nmae	Description
1	SGND	Shield Ground.
2	+5V	+5 volt power supply.
3	GND	Power and Signal ground.
4	X1	Horizontal analog input, PDL (1) in BASIC.
5	SW2	Joystick switch 2, orange button.
6	+12V	+12 volt power supply.
7	GND	Power and signal ground.
8	Y1	Vertical analog input, PDL (3) in BASIC.
9	SWO	Joystick switch zero.

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THE KEYBOARD

The keyboard is different in design but the locations of the Keyboard Data Input and the Clear Keyboard Strobe are the same. For more information see "THE KEYBOARD" in chapter 1.

CASSETTE INTERFACE JACKS

There are no cassette interface jacks in the Apple ///.

POWER CONNECTOR

The power connector is different but is not user accessible.

SPEAKER

The speaker is identical to the Apple][.

PERIPHERAL CONNECTORS

The Apple][emulation redefines a few of the pins on the connector and adds several new ones.

The most significant difference is that interrupts will not be sent to the 6502 from the slots. In fact the IRQ (pin 30) is an input to the cpu so the card can't even determine if an interrupt is occuring. Thus Emulation mode runs without interrupts, period.

The RES (pin 31) is an output to the card and goes low when the RESET key is pressed on the keyboard. However the microprocessor is actually performing an NMI not a RESET.

Peripheral Connector Pinout

GND	26	25	+5V
DMAOK	27	24	NOT USED
$\overline{\text{DMAI}}$	28	23	NOT USED
$\overline{\text{IONMI}}$	29	22	$\overline{\text{TSADE}}$ (Open collector)
$\overline{\text{IRQ}}$	30	21	RDY (Open collector)
$\overline{\text{IORES}}$	31	20	$\overline{\text{I/O STROBE}}$
$\overline{\text{INH}}$	32	19	PH0
-12V	33	18	R/$\overline{\text{W}}$
-5V	34	17	A15
SYNC	35	16	A14
C7M	36	15	A13
Q3	37	14	A12
$\overline{\text{C1M}}$	38	13	A11
$\overline{\text{IOCLR}}$	39	12	A10
C1M	40	11	A9
$\overline{\text{DEV SEL}}$	41	10	A8
D7	42	9	A7
D6	43	8	A6
D5	44	7	A5
D4	45	6	A4
D3	46	5	A3
D2	47	4	A2
D1	48	3	A1
D0	49	2	A0
+12V	50	1	$\overline{\text{I/O SELECT}}$

Peripheral Connector Signal Description

Pin:	Name:	Description:
1	$\overline{\text{I/O SELECT}}$	This line, normally high, will become low when the microprocessor references page $Cn, where n is the individual slot number. This signal become active during PH0 (nominally 500ns) and will drive 12 LSTTL loads.
2-17	A0-A15	The buffered address bus. The address on these lines becomes valid within 300ns after the beginning of $\overline{\text{C1M}}$ and remains vaild through PH0. These lines will each drive 8 LSTTL loads.
18	R/$\overline{\text{W}}$	Buffered Read/$\overline{\text{Write}}$ signal. This becomes valid at the same time the address bus does, and goes high during a read cycle and low during a write. This line can drive up to 10 LSTTL loads.
19	PH0	A 1 MHz signal which is identical to C1M. This line will drive 5 LSTTL inputs.
20	$\overline{\text{I/O STROBE}}$	This line will go low during C1M when the address bus contains an address between $C000 and $CFFF. This line will drive 12 LSTTL loads.
21	RDY	The 6502's RDY input. This line should change only during C1M, and when low will halt the microprocessor on the next read cycle. This line has a 1K ohm pullup to +5V. This line should be driven from an open collector output.
22	$\overline{\text{TSADB}}$	A low on this line from the peripheral will cause the address bus to tri-state for Direct Memory Access (DMA) applications. This has a 1 K ohm resistor pullup to +5V. This should be driven from an open collector output.
23		Not used in an Apple ///.
24		Not used in an Apple ///.
25	+5V	Positive 5-volt supply, 2.0 amps total for all peripheral boards together (but note a limit of 1.5 Watts per board).
26	GND	System circuit ground. 0 volt line from power supply. Do not use for shield ground.
27	DMAOK	Acknowledge signal to the peripheral following

		its request for the special Direct Memory Access (DMA) mode. Informs the peripheral that the DMA can now proceed.
28	$\overline{\text{DMAI}}$	Direct Memory Access (DMA) interrupt. Requests the A Apple /// DMA mode. Has a 1 K ohm pullup to +5. This should be driven from an open collector output.
29	$\overline{\text{IONMI}}$	Input/Output Non-Maskable Interrupt. This is equivalent to the IORES (pin 31) line as it will execute the same code in the Autostart ROM. This line should be driven by an open collector output.
30	$\overline{\text{IRQ}}$	This line is ignored in Apple][emulation mode. It should be driven by a TTL output.
31	$\overline{\text{IORES}}$	Input/Output Reset signal used to reset the peripheral devices. Pulled low by a power on or RESET key. This line will drive 12 LSTTL loads.
32	$\overline{\text{INH}}$	Inhibit line. When a device pulls this line low, all system memory is disabled. This line has a 1 K ohm pullup resistor to +5V and should be driven form an open collector output.
33	-12V	Negative 12 volt supply, 200mA total for all peripheral boards together.
34	-5V	Negative 5 volt supply, 200mA total for all periperal boards together.
35	SYNC	The 6502 opcode synchronization signal. Can be used for external bus control signals. Will drive 10 LSTTL loads.
36	C7M	Seven MHz high frequency clock. Will drive 10 LSTTL loads.
37	Q3	A 2MHz (nonsymetrical) general purpose timing signal. Will drive 10 LSTTL inputs.
38	$\overline{\text{C1M}}$	Complement of C1M clock. This will drive 12 LSTTL loads.
39	$\overline{\text{IOCLR}}$	Provides the $C800 space disable function directly without address decoding ($CFFF is used for Apple][peripherals. It is addressed from $C02x. This line will drive 12 LSTTL loads.
40	$\overline{\text{C1M}}$	Phase C1M clock. This is the same as the microprocessor's 1 MHz clock. This will drive 12 LSTTL loads.
41	$\overline{\text{DEVICE SELECT}}$	This line becomes acive (low) on each peripheral

		connector when the address bus is holding address between $C0n0 and $C0nF where n is the slot number plus $8. This line will drive 12 LSTTL loads.
42-49	D7-D0	The 8-bit system data bus. During a write cycle, data is set up by the 6502 less than 300ns after the beginning of $\overline{\text{C1M}}$. During a read cycle the 6502 expects data to be ready no less than 100ns before the end of $\overline{\text{C1M}}$. These lines will drive 8 LSTTL inputs.
50	+12V	Positive 12 volt supply, 300mA total for all peripheral boards together.

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ROM LISTINGS

APPLE][EMULATION MODE AUTOSTART ROM LISTING

The following is a listing of addresses which changed content in the Autostart ROM to eliminate cassette I/O, read joysticks, and redirect the NMI vector to the RESET code.

```
;       THE ACIA IS CAPABLE OF GENERATING INTERRUPTS IN EMULATION MODE.
;        IF IT DOES THE INTERRUPT RECEIVER SETS THE PROCESSOR INTERRUPT
;        INHIBIT BIT TO PREVENT THE SERVICING OF THIS INTERRUPT


FA49: 4C 10 FF          JMP IHBIRQS     ;JMP TO CODE TO INHIBIT INTERRUPTS

FF10: 68                PLA             ;GET PROCESSOR STATUS BYTE
FF11: 09 04             ORA #$04        ;SET INTERRUPT INHIBIT BIT
FF13: 48                PHA             ;PUT STATUS BYTE BACK ON STACK
FF14: A5 45             LDA $45         ;RESTORE ACCUMULATOR
FF16: 40                RTI             ;RETURN WITH INTERRUPTS INHIBITTED


;       THE RESET KEY IN EMULATION MODE GENERATES AN NMI (NONMASKABLE
;        INTERRUPT).  THEREFORE THE NMI VECTOR IS SET TO POINT AT THE
;        RESET CODE WHICH ALSO MAKES SURE THE DISK MOTOR STOPS


FFFA: 62 FA             DFB     RESET   ;POINT NMI VECTOR TO RESET CODE

FA62: D8        RESET   CLD             ;BINARY ARITHMATIC PLEASE
FA63: AD EE C0          LDA     $C0EE   ;SET DISK READ
FA66: AD EC C0          LDA     $C0EC
FA69: AD E8 C0          LDA     $C0E8   ;TURN OFF DISK
FA6C: 20 84 FE          JSR     SETNORM
FA6F: 20 2F FB          JSR     INIT
FA72: 20 93 FE          JSR     SETVID
FA75: 20 89 FE          JSR     SETKBD
FA78: EA                NOP
FA79: EA                NOP
FA7A  EA                NOP


;       THE CASSETTE READ ROUTINE SIMPLY RETURNS TO USER CALLS
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```
FEFD: 60        READ    RTS     ;NO CASSETTE PORT - RETURN TO USER

FEFE-FF0A: EA           NOP     ;FILL CODE WITH NOPS
FF0B: 22
FF0C-FF0F: 00           BRK     ;STOP USER FROM JUMPING INTO MIDDLE OF CODE
FF17-FF2C: 00           BRK


;       THE CASSETTE WRITE ROUTINE SIMPLY RETURNS TO USER CALLS


FECD: 60                RTS     ;NO CASSETTE PORT - RETURN TO USER

FECE-FEF2: EA           NOP     ;FILL CODE WITH NOPS
FEF3-FEF5: 00           BRK     ;STOP USER JUMPING INTO CODE


;       READ JOYSTICK AXIS.  THIS IS THE SAME ENTRY ADDRESS OF PREAD
;        WHICH READS THE GAME PADDLES IN THE APPLE ][
;
;       X REGISTER CONTAINS JOYSTICK AXIS AND Y RETURNS $00-$FF OF JOYSTICK
;
;               X REGISTER      JOYSTICK AXIS
;
;                   0           PORT A, X AXIS
;                   1           PORT B, X AXIS
;                   2           PORT A, Y AXIS
;                   3           PORT B, Y AXIS


FB1E: 8A        PREAD   TXA             ;SAVE X REGISTER
FB1F: 48                PHA
FB20: 49 01             EOR #$01        ;REMAP JOYSTICK ADDRESS
FB22: AA                TAX
FB23: AD 59 C0          LDA $C059       ;SET ANALOG MUX TO PORT B, X AXIS
FB26: AD 5E C0          LDA $C05E
FB29: AD 5A C0          LDA $C05A
FB2C: 4C C9 FC          JMP JOY2

FCC9: E8        JOY2    INX
FCCA: CA                DEX             ;SET FLAGS
FCCB: F0 12             BEQ JOY3        ;PORT B, X AXIS?
FCCD: AD 5F C0          LDA $C05F       ;NO
FCD0: CA                DEX
FCD1: F0 0C             BEQ JOY3        ;PORT A, X AXIS?
FCD3: AD 58 C0          LDA $C058       ;NO
FCD6: CA                DEX
FCD7: F0 06             BEQ JOY3        ;PORT B, Y AXIS?
FCD9: AD 5E C0          LDA $C05E       ;NO
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```
FCDC: AD 5B C0          LDA $C05B       ;MUST BE PORT A, Y AXIS
FCDF: AD 5C C0  JOY3    LDA $C05C       ;CHARGE CAPACITOR
FCE2: A9 0F             LDA #$0F        ;WAIT 800US
FCE4: 20 A8 FC          JSR WAIT
FCE7: A0 80             LDY #$80
FCE9: AD 5D C0          LDA $C05D       ;START TIMEOUT
FCEC: A2 48             LDX #$48        ;WAIT 370US
FCEE: CA        JOY4    DEX
FCEF: 10 FD             BPL JOY4
FCF1: E8        JOY5    INX
FCF2: B9 E6 BF          LDA $BFE6,Y     ;FALSE READ
FCF5: 2A                ROL
FCF6: AD 66 C0          LDA $C066       ;BIT 7 IS VOLTAGE CROSSOVER
FCF9: 30 F6             BMI JOY5        ;HAS VOLTAGE CROSSED OVER?
FCFB: 8A                TXA             ;YES
FCFC: 10 04             BPL JOY6        ;WAS COUNT POSITIVE?
FCFE: A9 FF             LDA #$FF        ;NO
FD00: D0 01             BNE JOY7        ;USE $FF
FD02: 2A        JOY6    ROL             ;DOUBLE COUNT
FD03: A8                TAY             ;RETURN COUNT IN Y
FD04: 68                PLA             ;RESTORE X
FD05: AA                TAX
FD06: 60                RTS

FD07-FD0B: 00           BRK             ;FILL SPACE
```