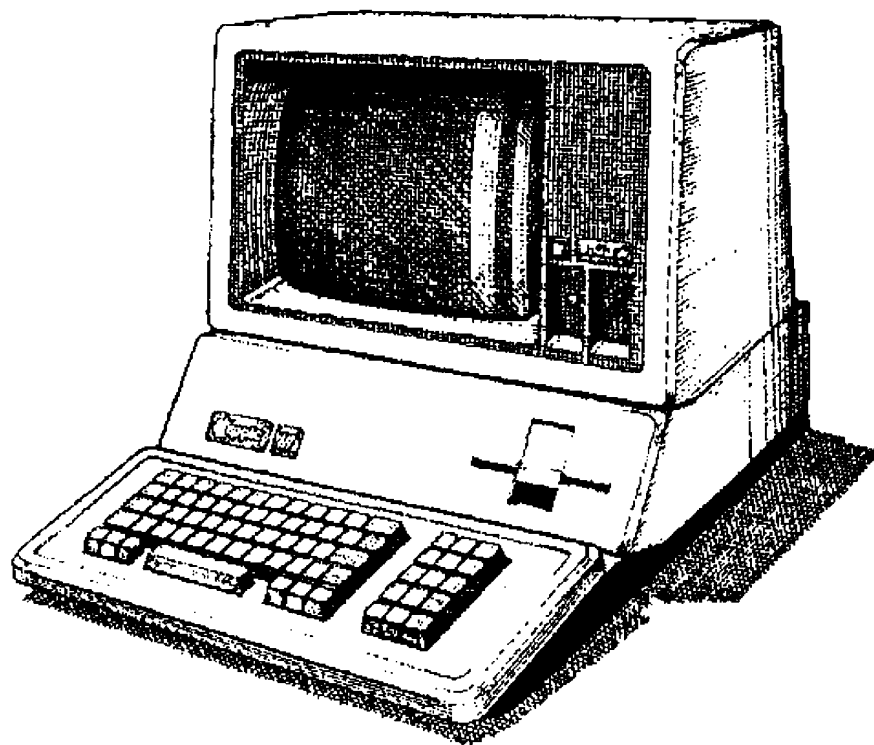




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




Section I of II • Theory of Operation

Chapter 11 • Schematic Diagrams

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-  = 750
-  = ALL UNITS UNDER TEST MOLEX PINS TO BE LOCATED TOGETHER.
-  = ALL TIMING MOLEX PINS TO BE LOCATED TOGETHER.
- THIS SCHEMATIC REPRESENTS ASSY 610-C105 AT REV LEVEL 1 F.

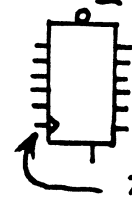
FOR STANDARD SYSTEMS G9 IS 341-0030, FOR EURO SYSTEMS G9 IS 341-0060.
 FOR STANDARD SYSTEMS Y1 IS H.316630 MHZ, FOR EURO SYSTEMS Y1 IS H.250450 MHZ.

REV	Q001	REV	REV	REV	REV	REV	REV	REV	REV
C2		C3		E		F		G	
ENG. RELEASE		PRE-PRODUCTION RELEASE		PRE-PRODUCTION CHANGES		ECO. ECO RELEASE		REV	
						DELETED CAP ARRAY (CR1), 4750 NIB, M13, K13, N13, N10 WAS PC NETWORK, C5 WAS 4750. G1 WAS G00 N.C. IS NOW 1050. J20, 7 WAS COLORHILL, J20, 9 WAS FORCAGE, DELETED MICROPROCESSOR (B3) -		H8 WAS L504J R15 WAS 4750 CHM, R16 WAS 750 CHM. ADDED 1K04M RESISTOR AT K10.	

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ITEM	QTY	PART NUMBER	DESCRIPTION																				
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MATERIALS	N/A	FINISH	N/A																				
ANGLES	N/A	FRAC.	N/A																				
DIMENSIONS	N/A	TOLERANCES	N/A																				
FRACTIONS	N/A	DIMENSIONS	N/A																				
TOLERANCES	N/A	DIMENSIONS	N/A																				
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TITLE	SCALE	SHEET 1	OF 10																				
SCHEMATIC APPLE /// MAIN LOGIC #2	NONE	1	1																				



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PAGE LOCATION

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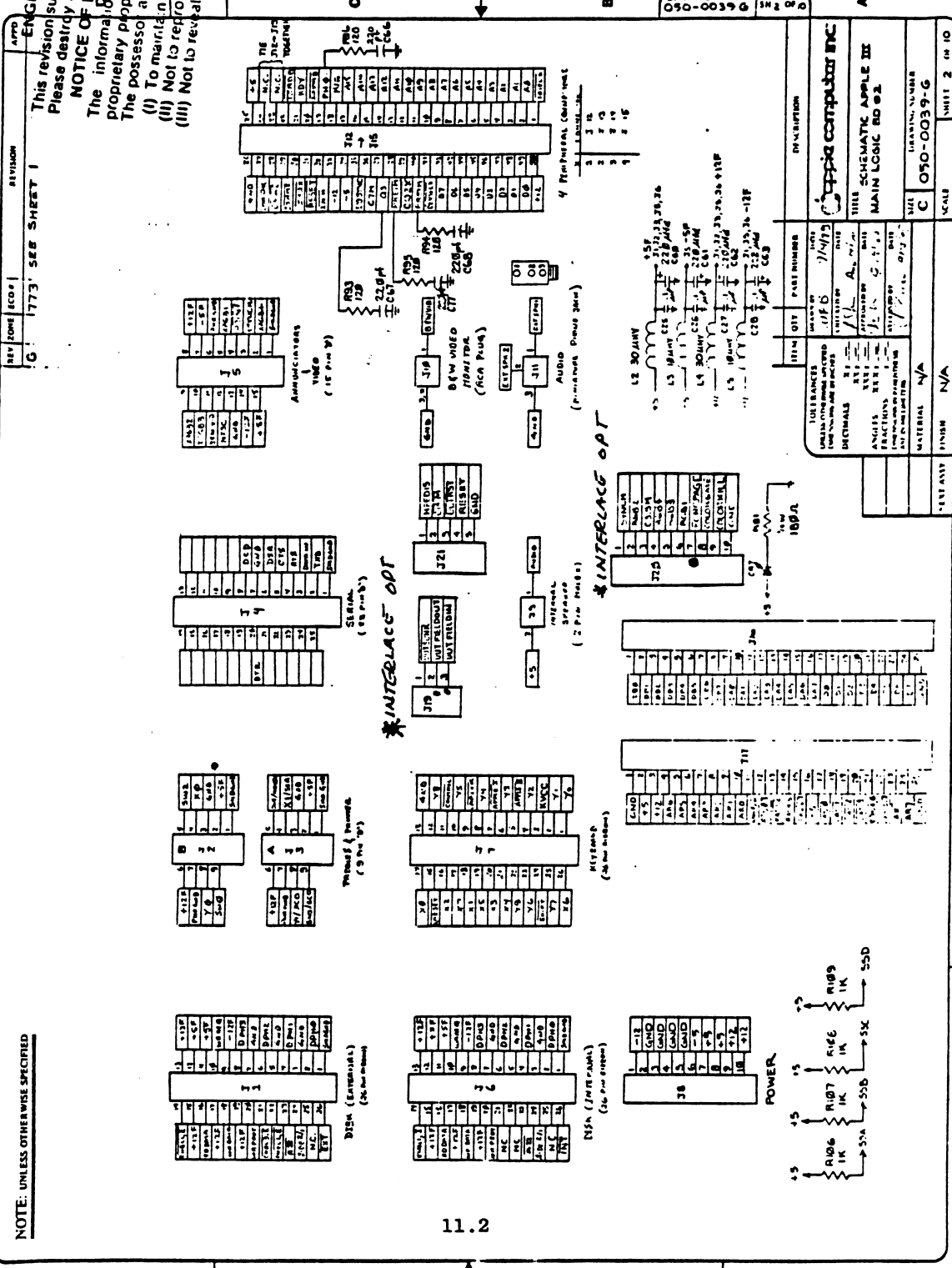
ALPHA NOMENCLATURE
LOCATION

Page
5 of 10

11.1

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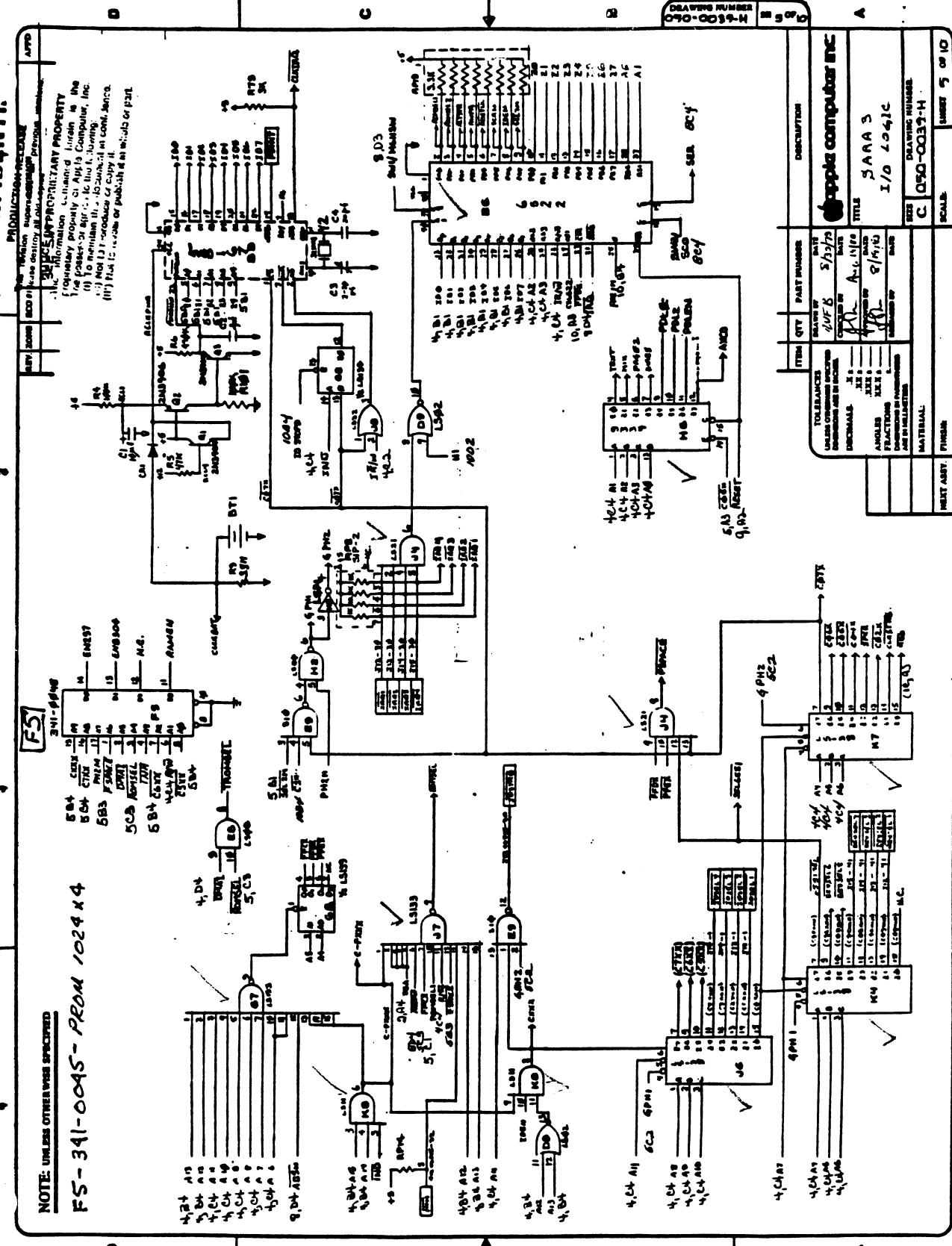
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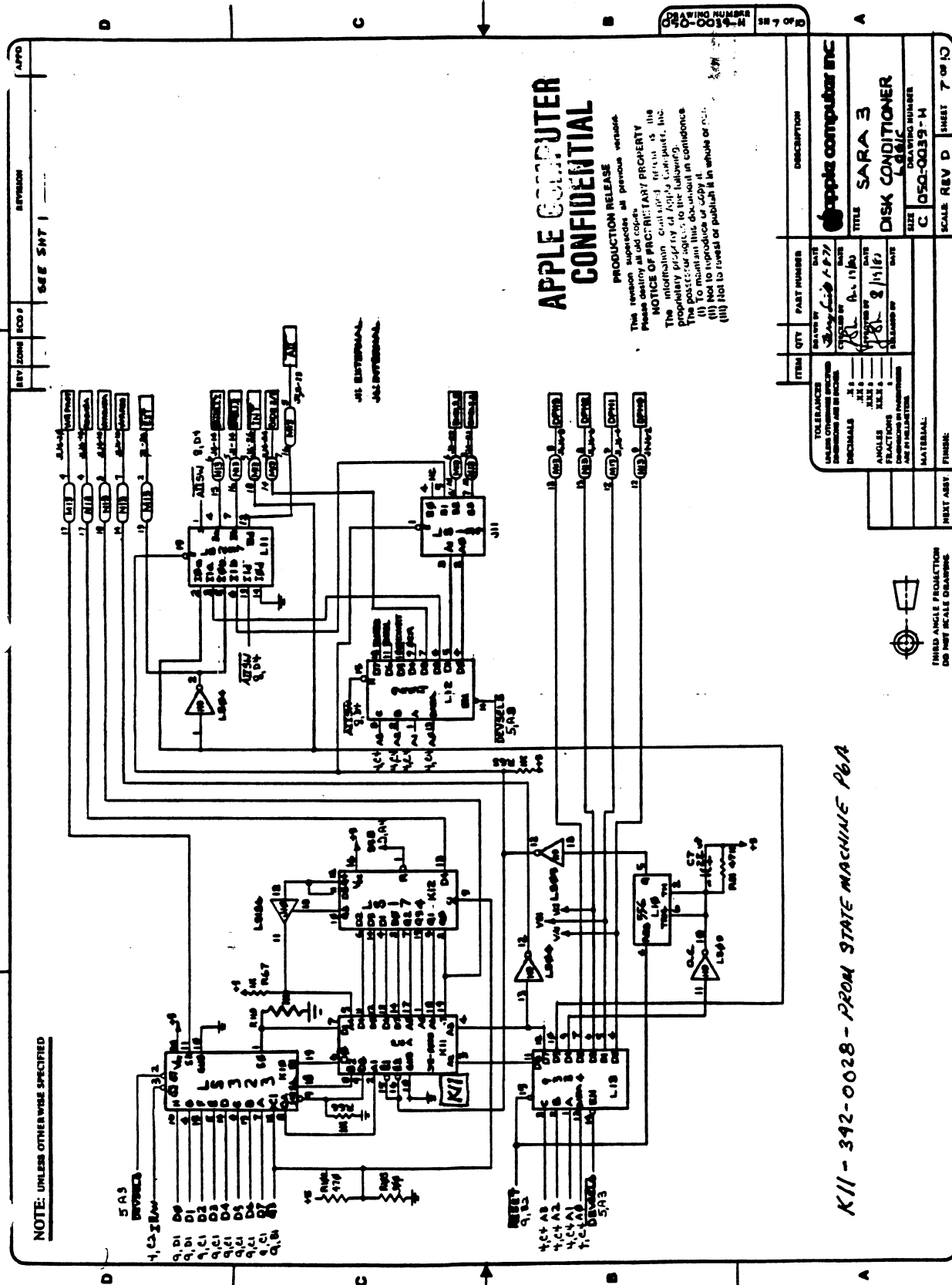
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FS-341-0045 - PROM 1024 X 4

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DRAWING NUMBER C 050-0039-H		SHEET 5 OF 10	
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4	1	74LS163	BINARY COUNTER
5	1	74LS164	8-BIT SHIFTER
6	1	74LS165	8-BIT SHIFTER
7	1	74LS166	8-BIT SHIFTER
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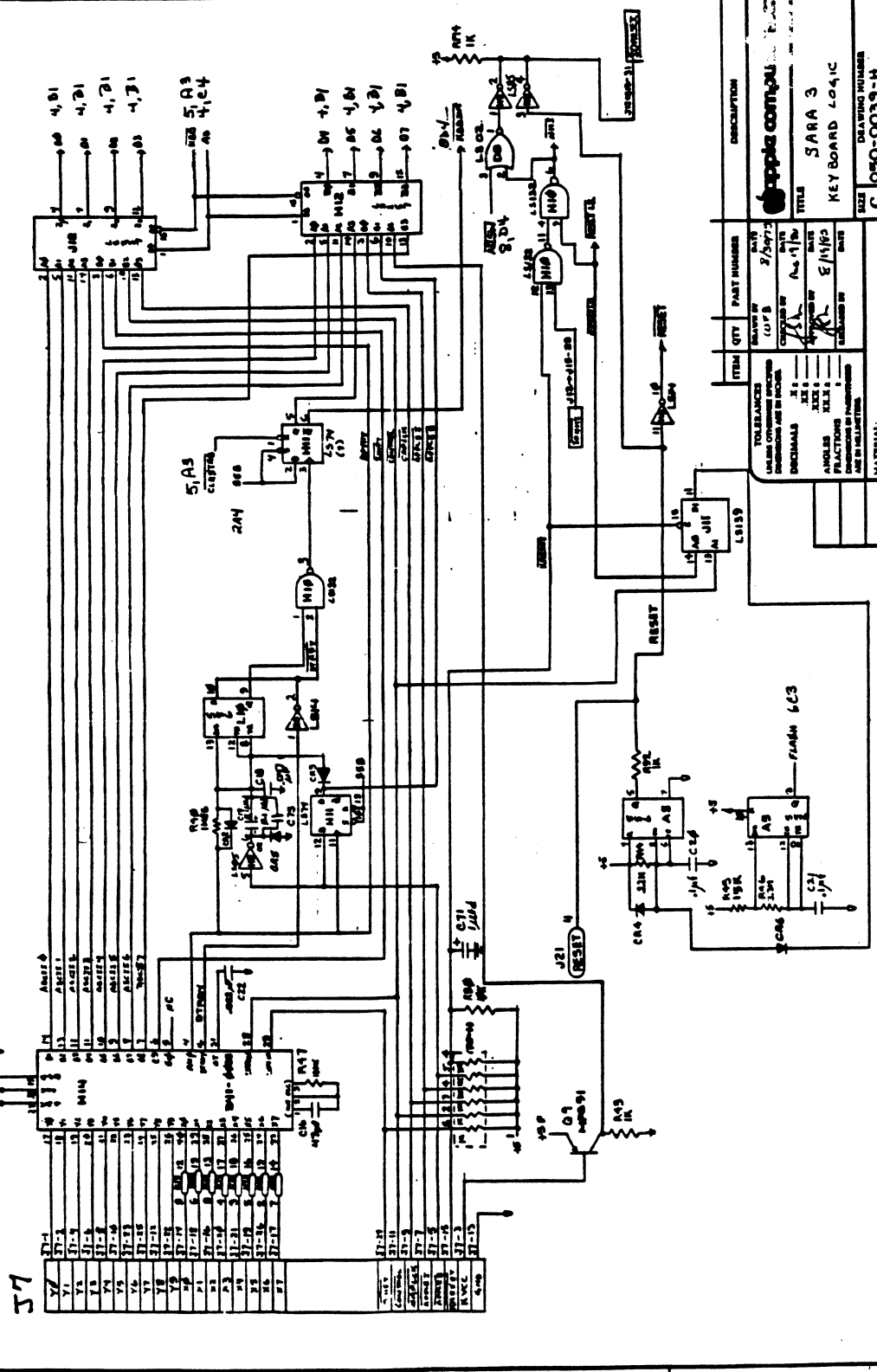
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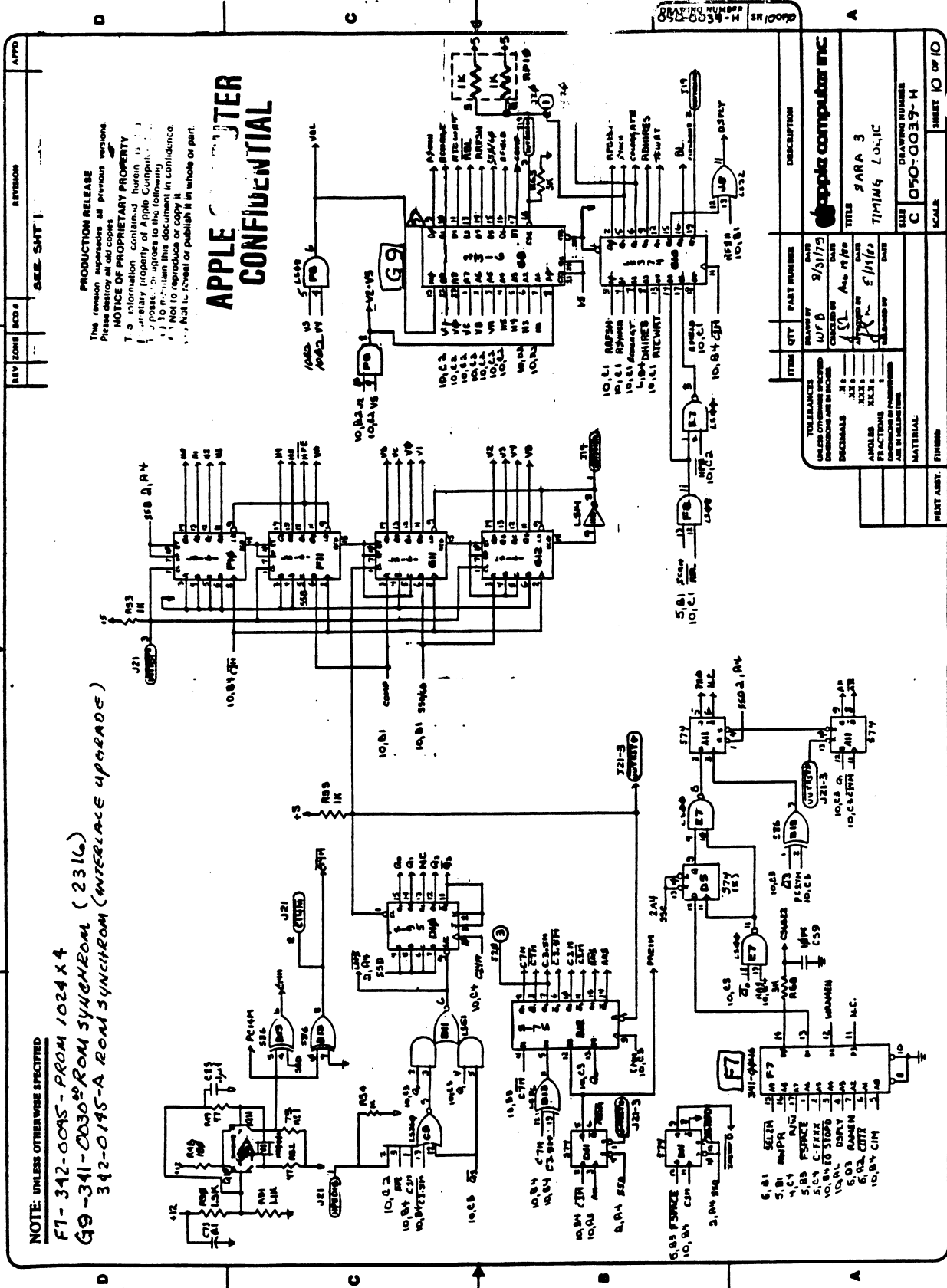
H14 - 342-0035 - ROM KEYBOARD ENCODER A3

NOTE: UNLESS OTHERWISE SPECIFIED



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U2	1	7805	7805 REGULATOR
R1	1	10K	10K RESISTOR
R2	1	10K	10K RESISTOR
C1	1	100UF	100UF CAPACITOR
J14	1	27P	27P CONNECTOR
J15	1	27P	27P CONNECTOR

DRAWING NUMBER C-050-0035-14	
TITLE SARA 3 KEYBOARD LOGIC	
DATE 5/11/80	DRAWING NUMBER C-050-0035-14
SCALE	SHEET 9 OF 10



NOTE: UNLESS OTHERWISE SPECIFIED

F7-342-00A5 - PROM 1024 X 4

G9-341-0030 ROM SYNCHROM (23LG)

342-0195-A ROM SYNCHROM (INTERLACE UPGRADE)

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Apple Computer Inc.
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 TIMING LOGIC

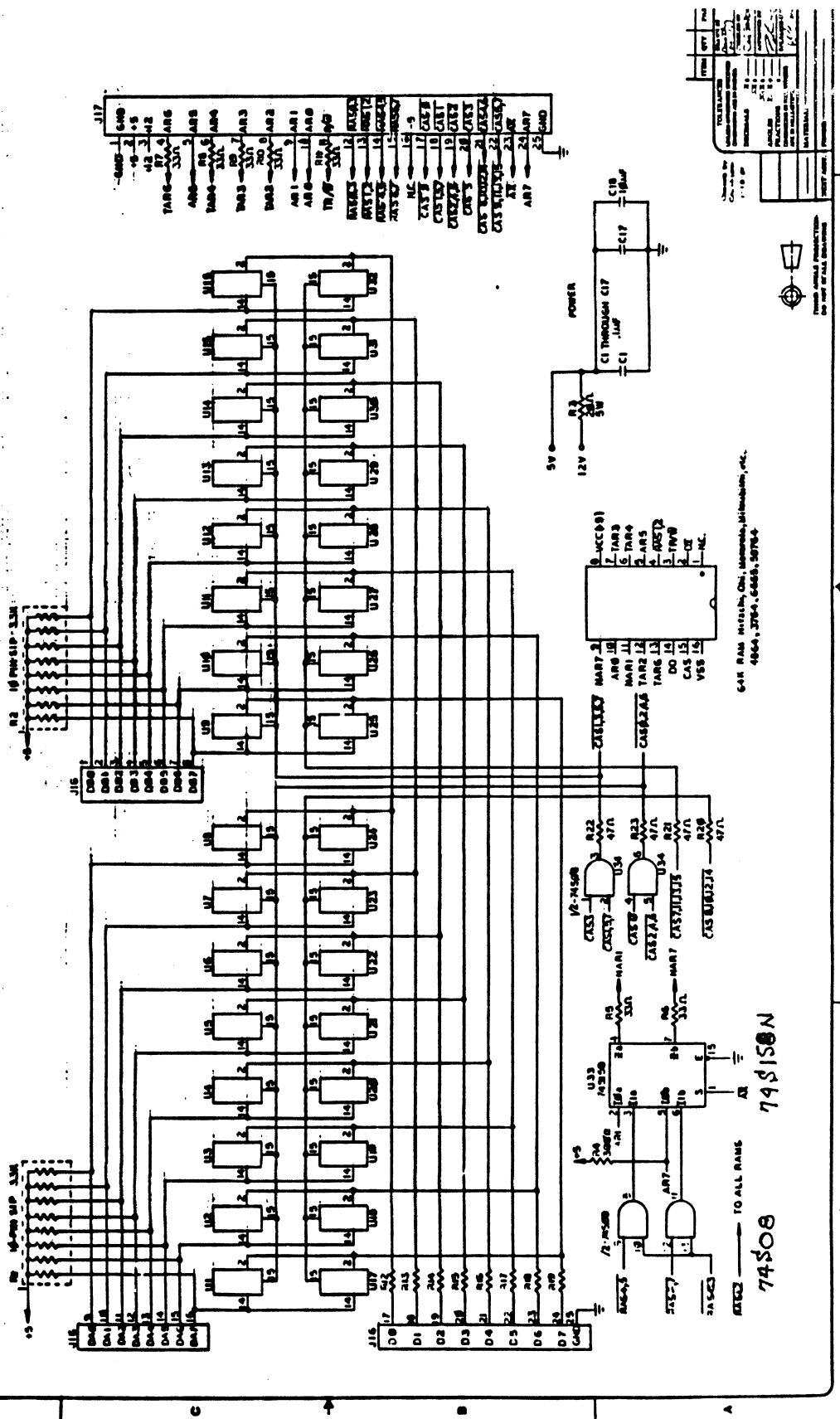
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 DRAWING NUMBER: C 050-0039-H

SCALE: 1
 SHEET 10 OF 10

REV	DATE
A	7/74
B	8/74
C	1/75

APPLE /// 5V MEMORY BOARD (PIN 610-8101)

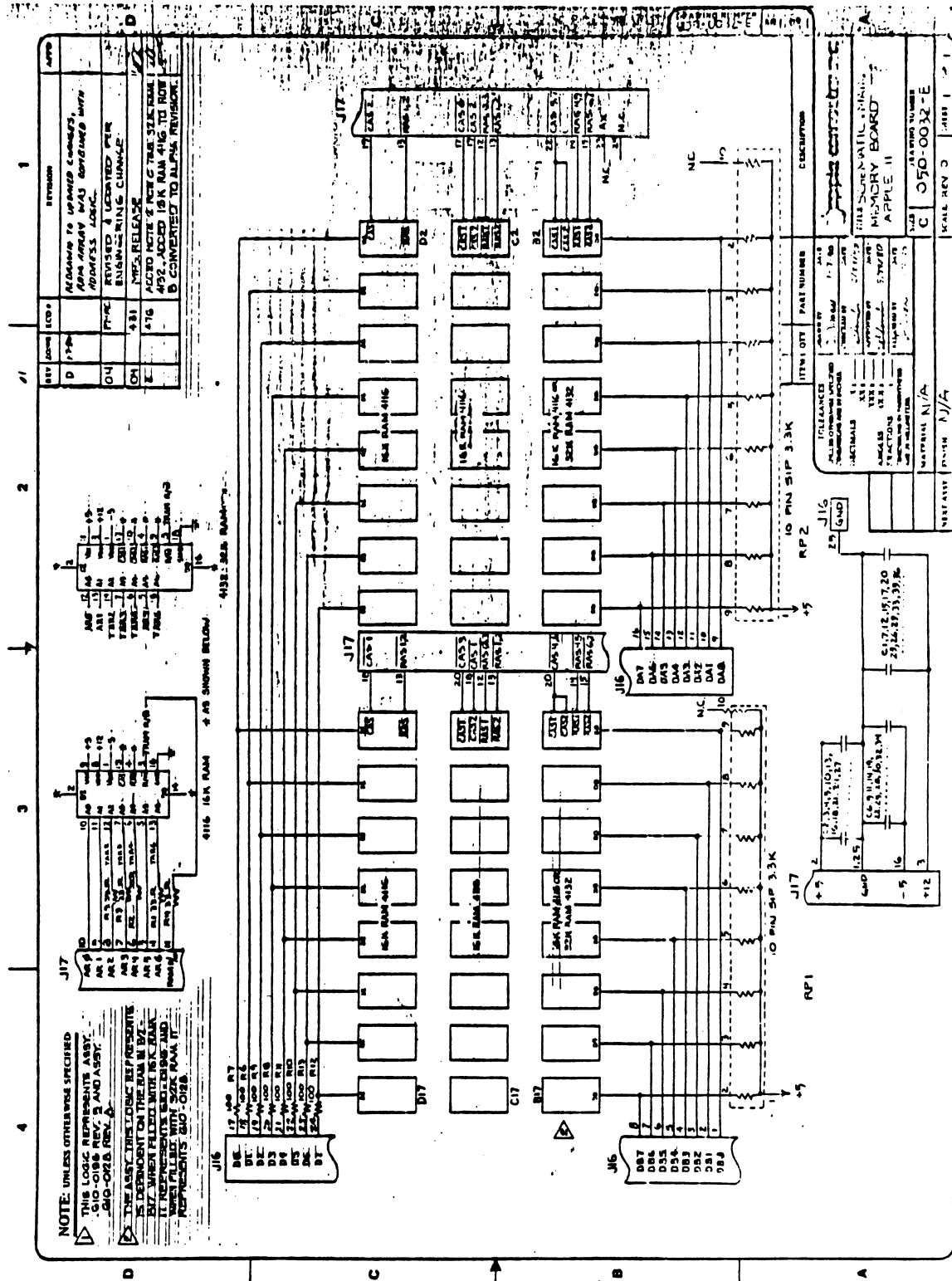
NOTE: THIS BOARD OPERATES AT 5V. THROUGH BOARD: 100 Ω.



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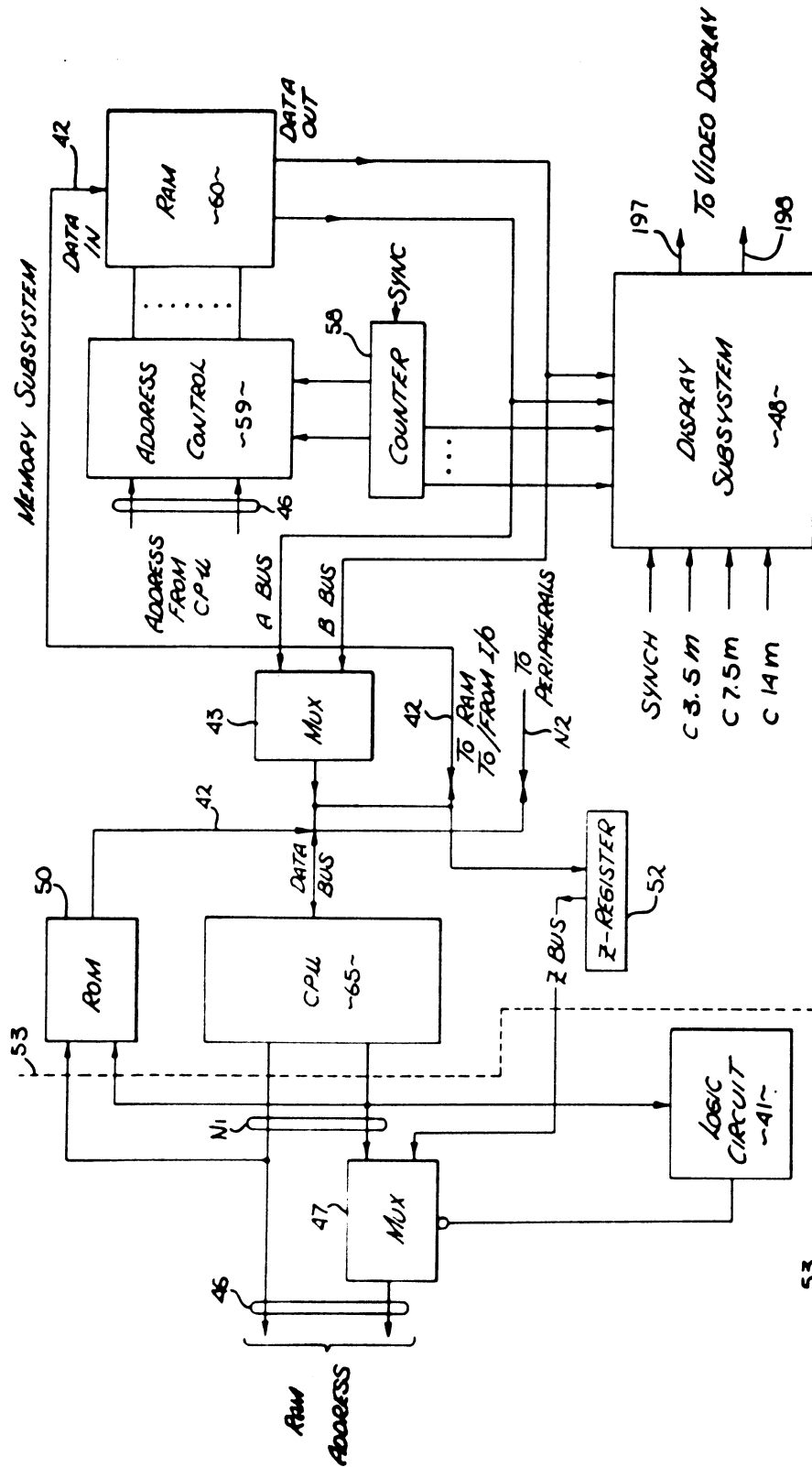
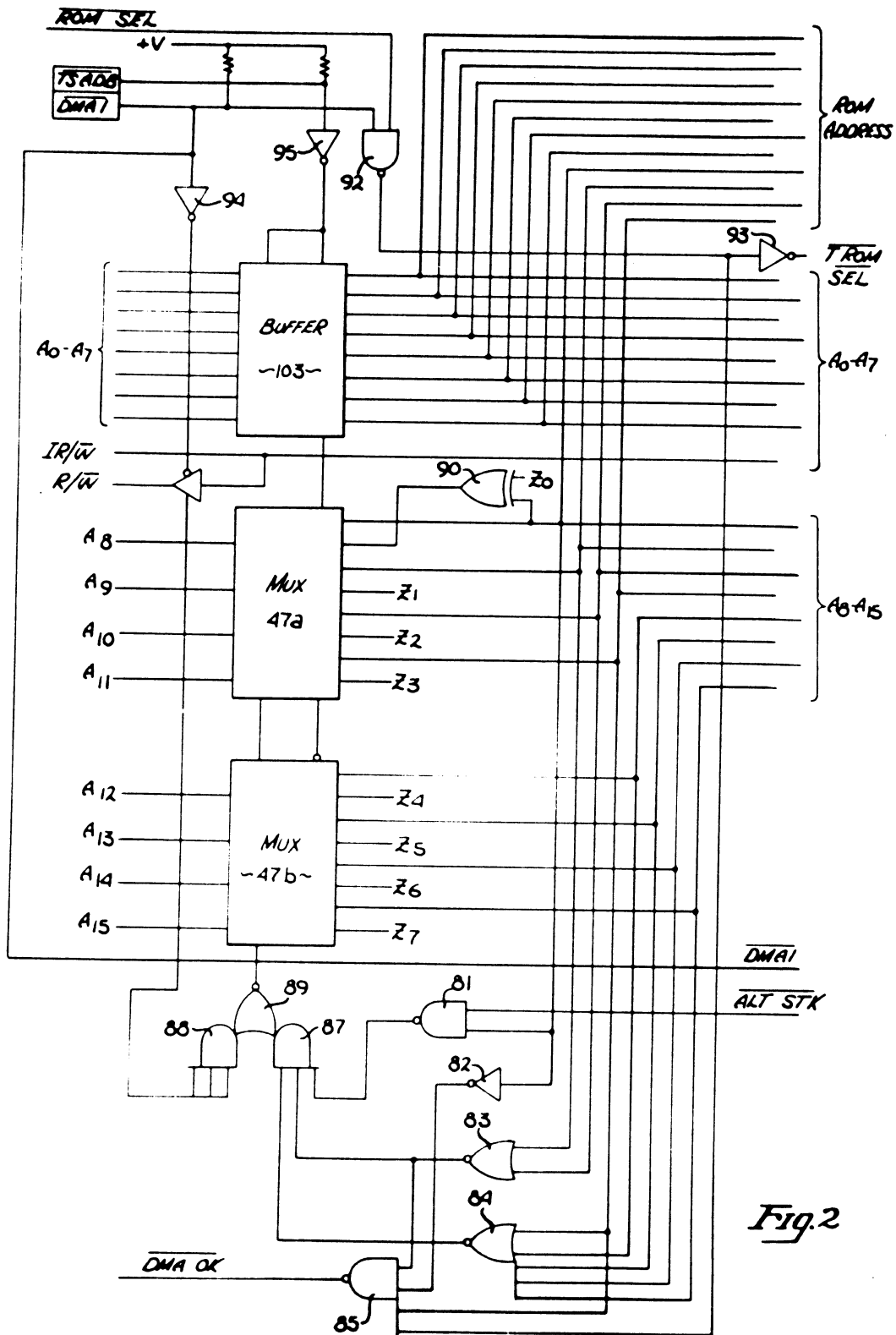


Fig. 2

MAJOR COMPONENTS and SUBSYSTEMS

Source /// PATENT - MAY 1983



ADDRESS and DATA BUS ARCHITECTURE

Source */// PATENT - MAY 1983*

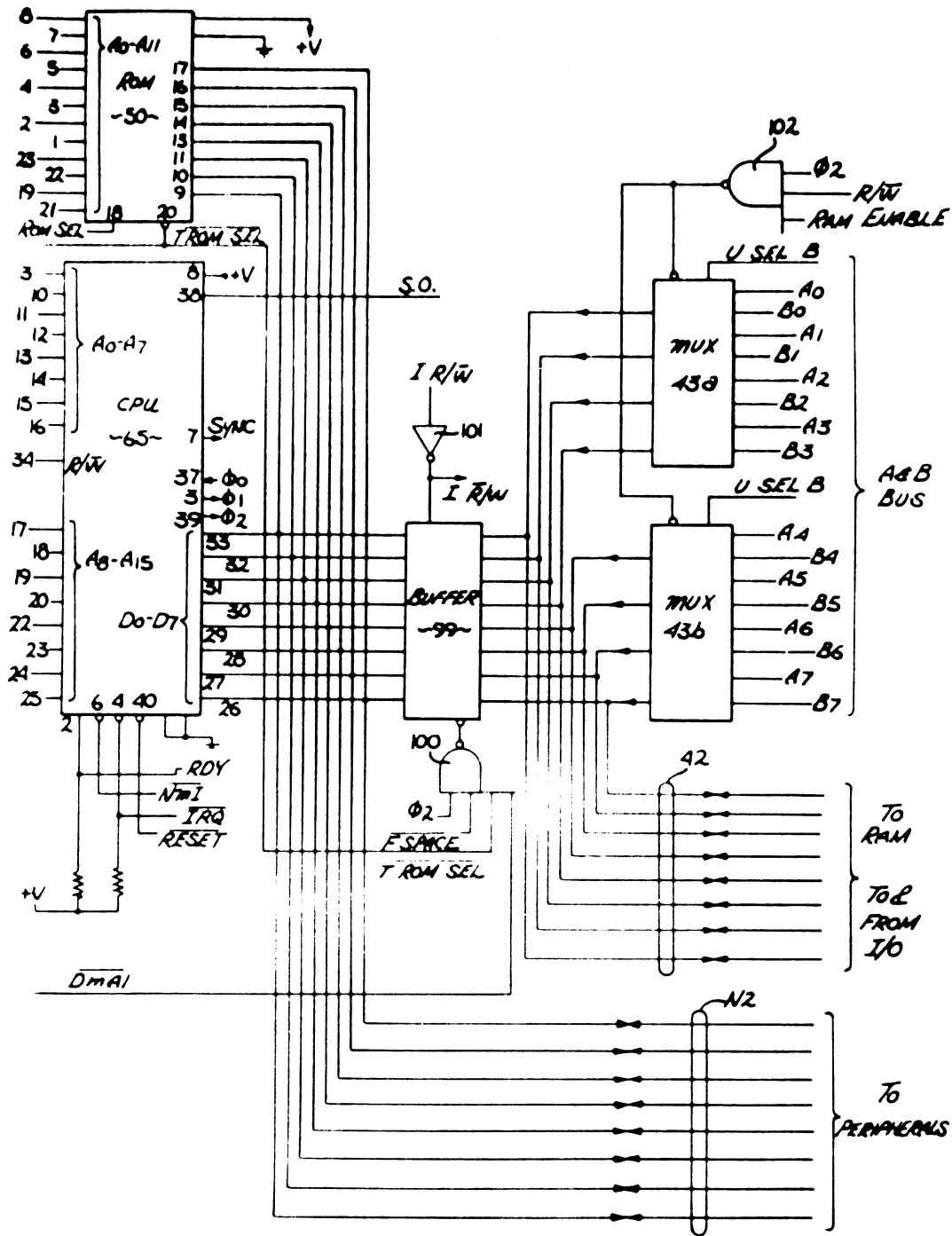


Fig. 3

CPU and ADDRESS/DATA BUS INTERFACE

Source /// PATENT - MAY 1983

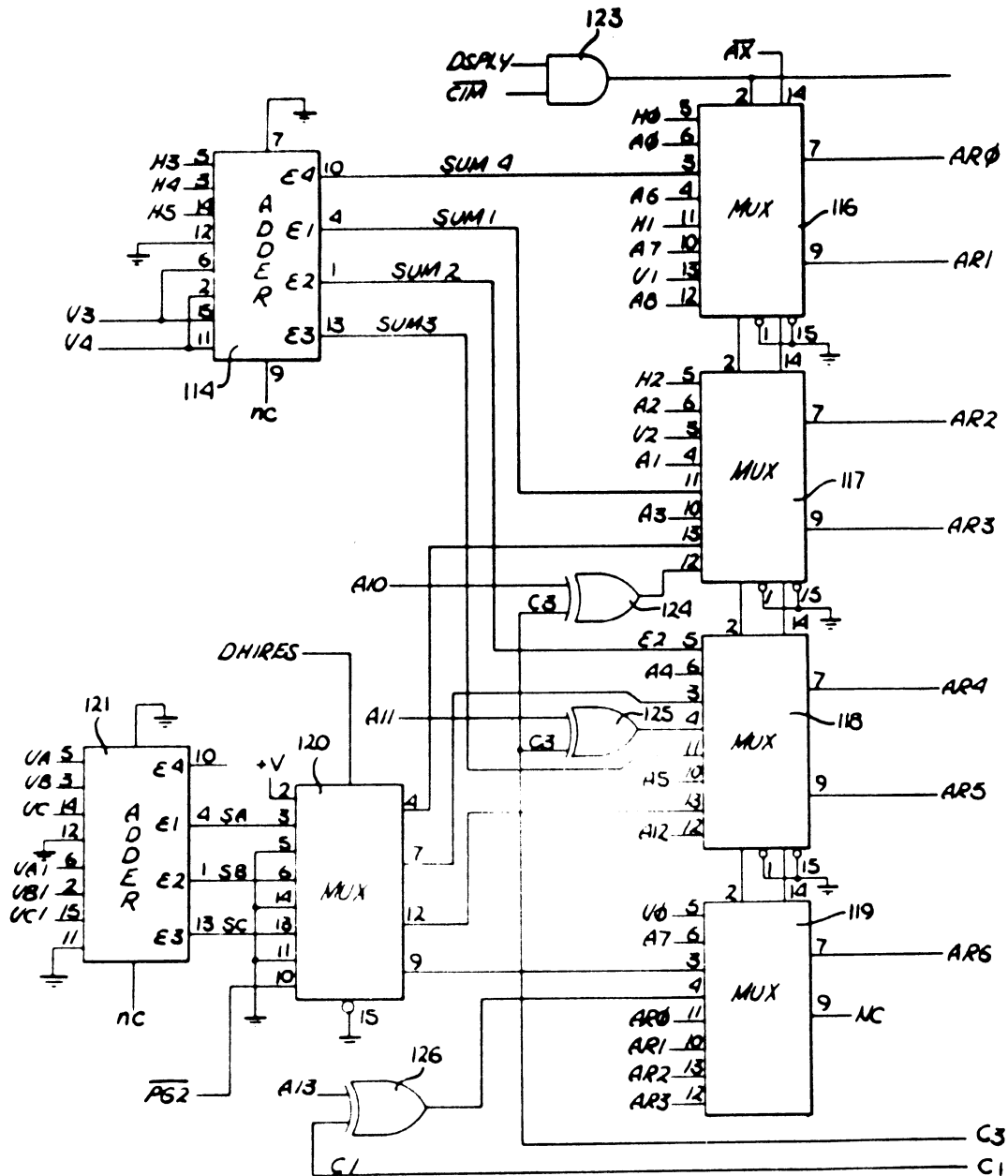
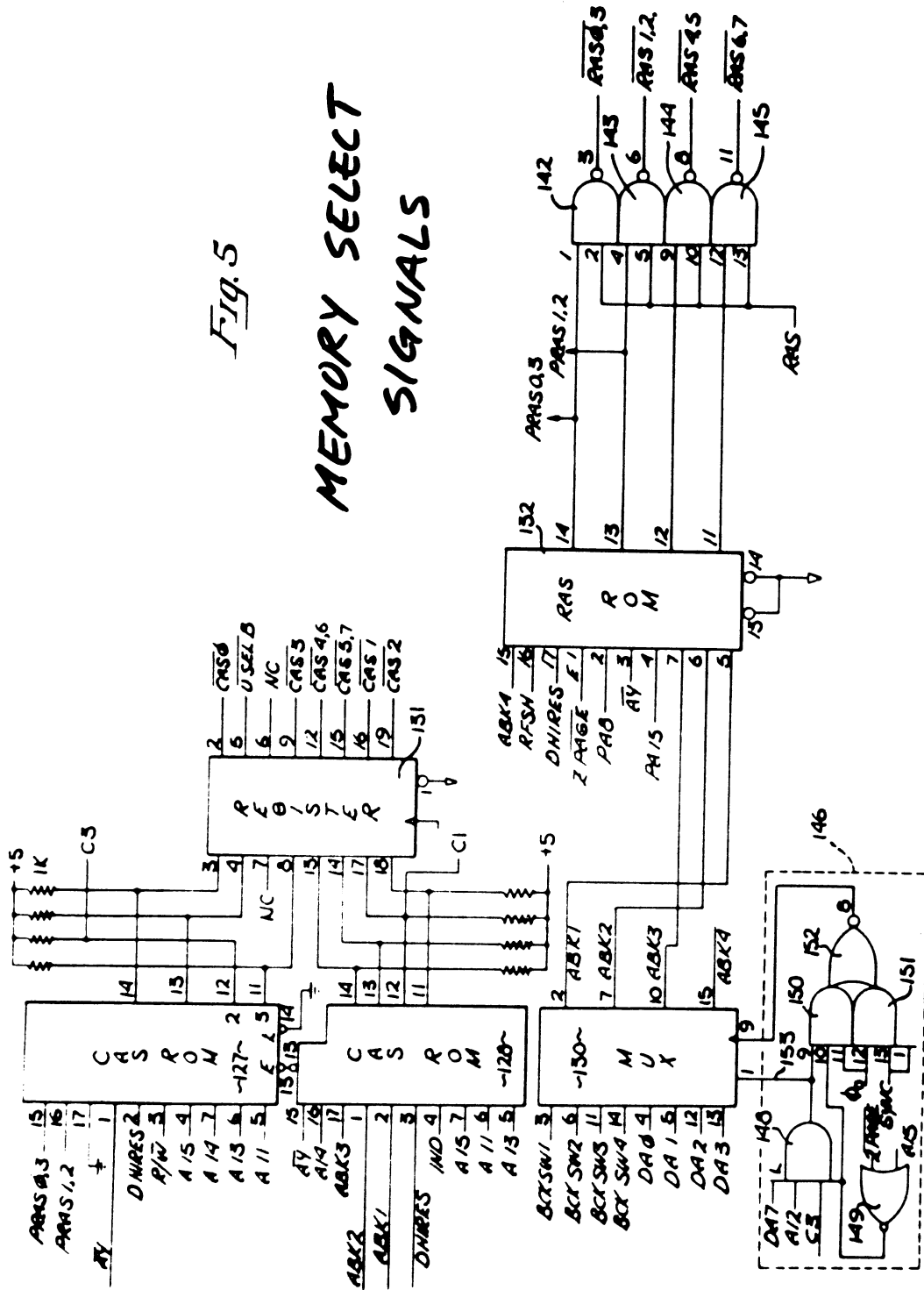


Fig. 4

**ADDRESS BUS and DISPLAY COUNTER
SIGNAL SELECTION CIRCUITRY**

Source III PATENT—MAY 1983

FIG. 5
MEMORY SELECT SIGNALS



Source /// PATENT - MAY 1983

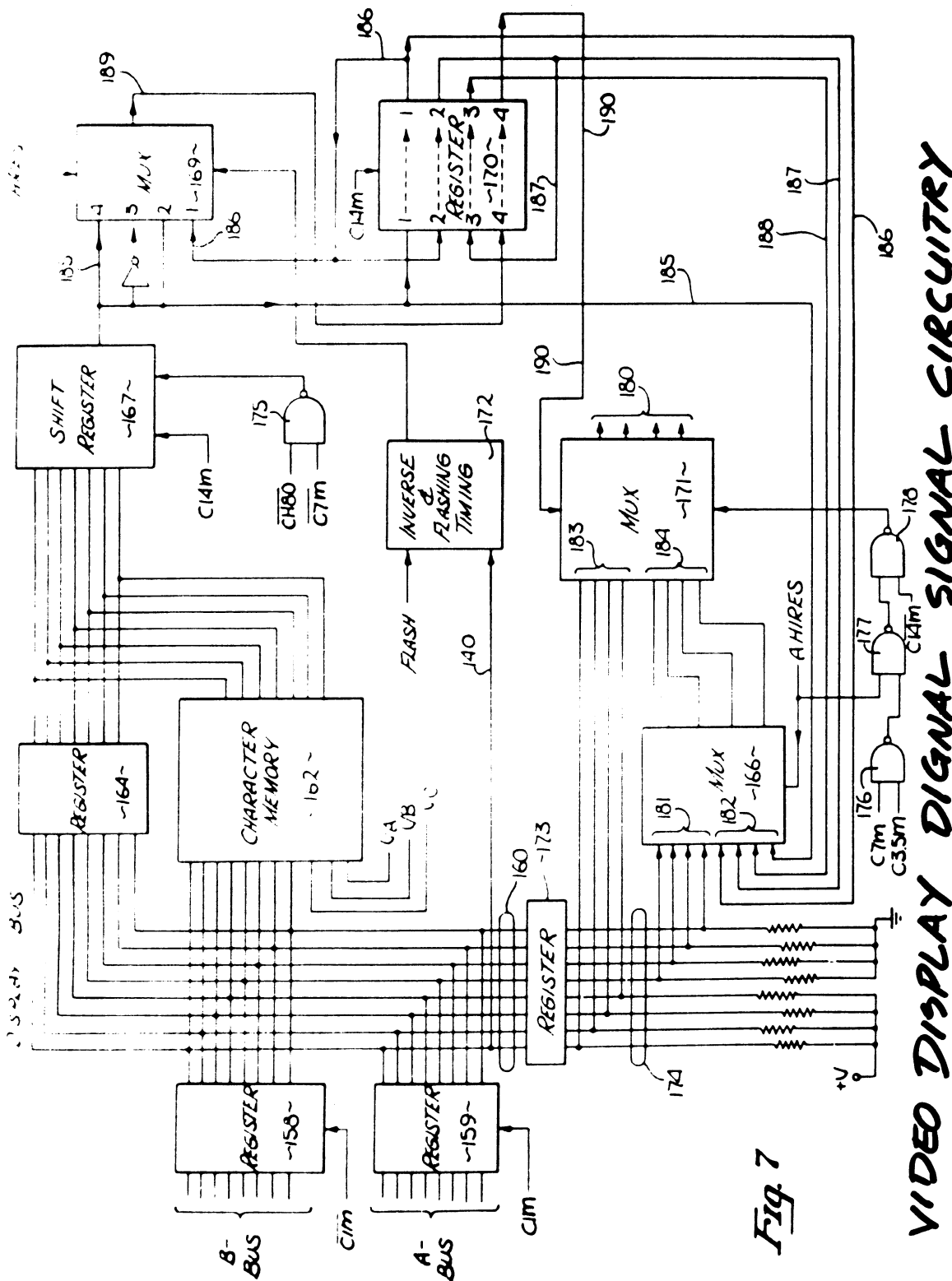


Fig. 7

VIDEO DISPLAY SIGNAL CIRCUITRY

Source III PATENT - MAY 1983

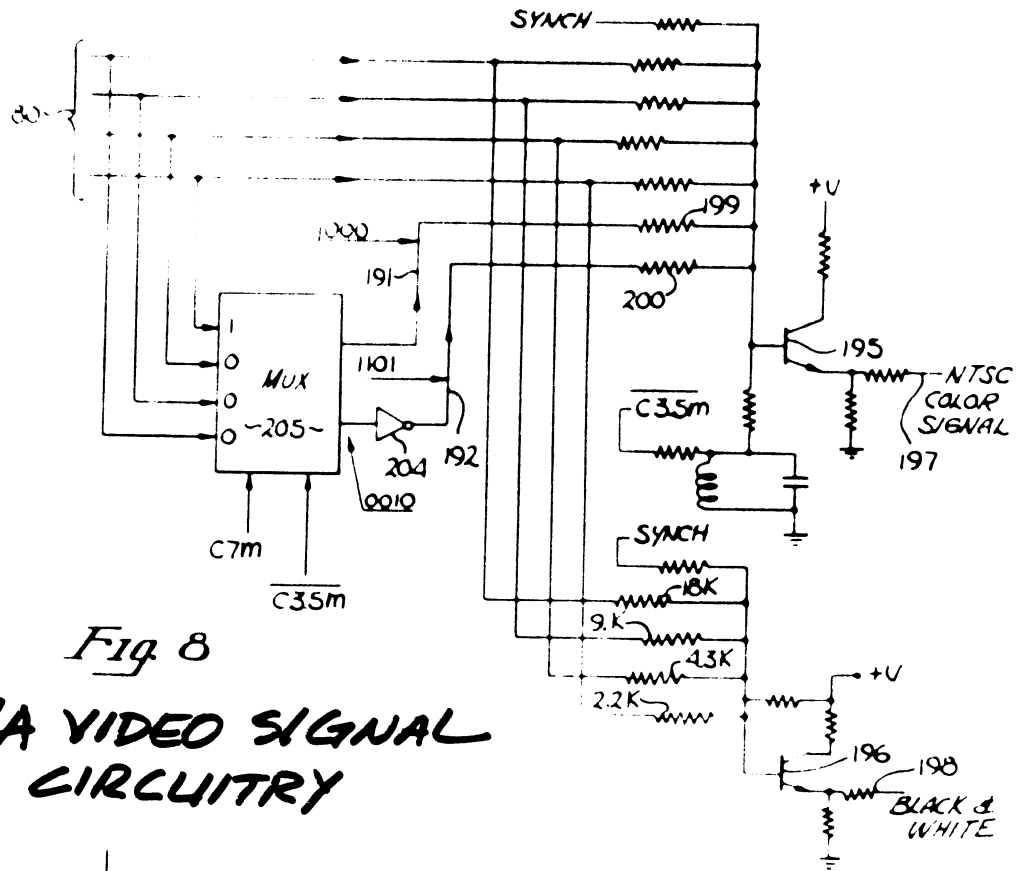
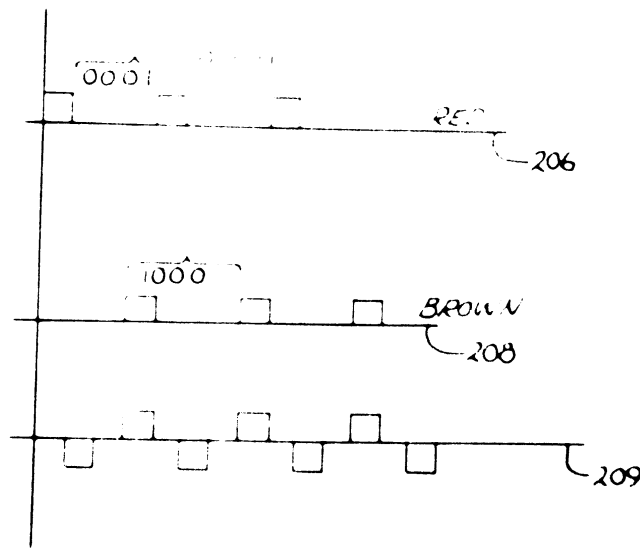


Fig 8
**D/A VIDEO SIGNAL
 CIRCUITRY**



VIDEO SIGNALS

Fig. 9

Source /// PATENT - MAY 1983

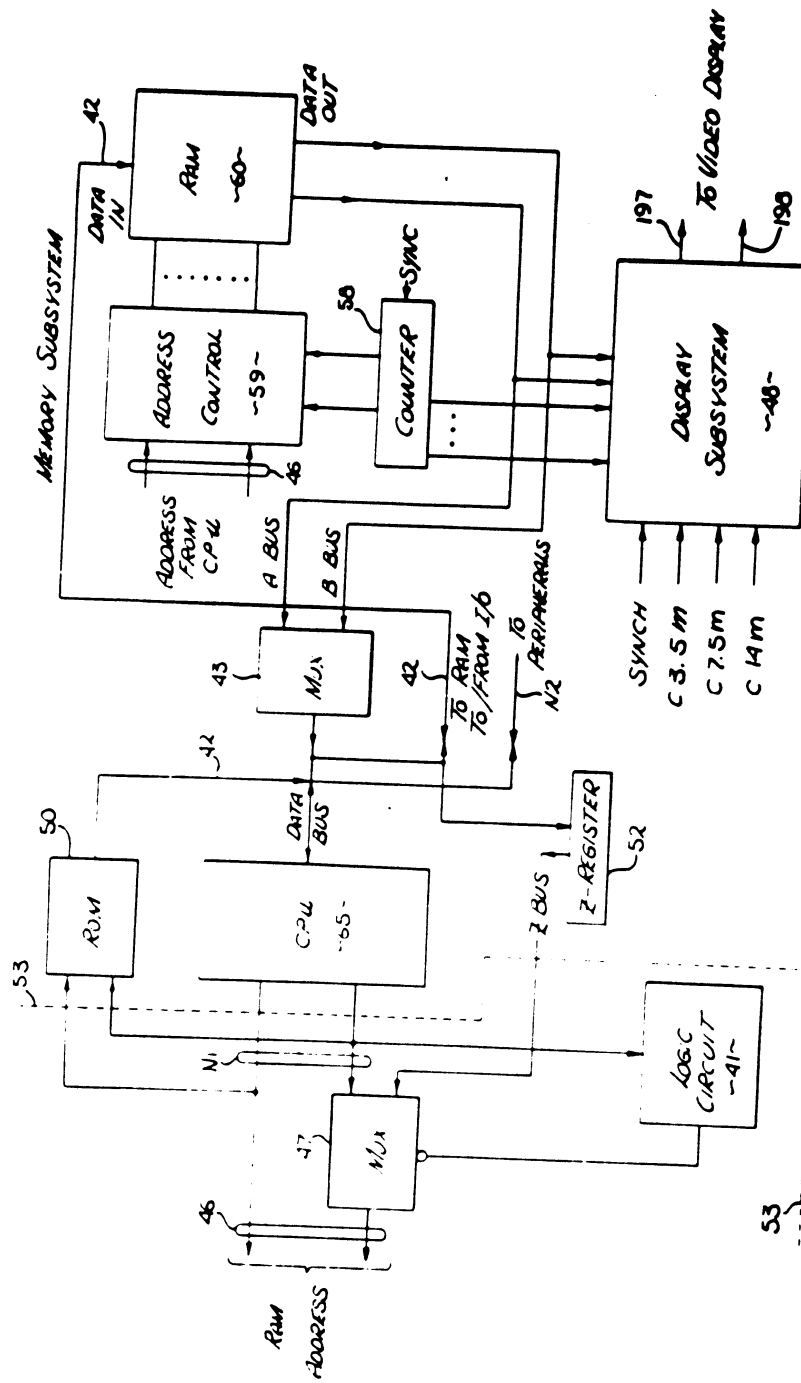


Fig. 1

Source III PATENT - AUG 1985

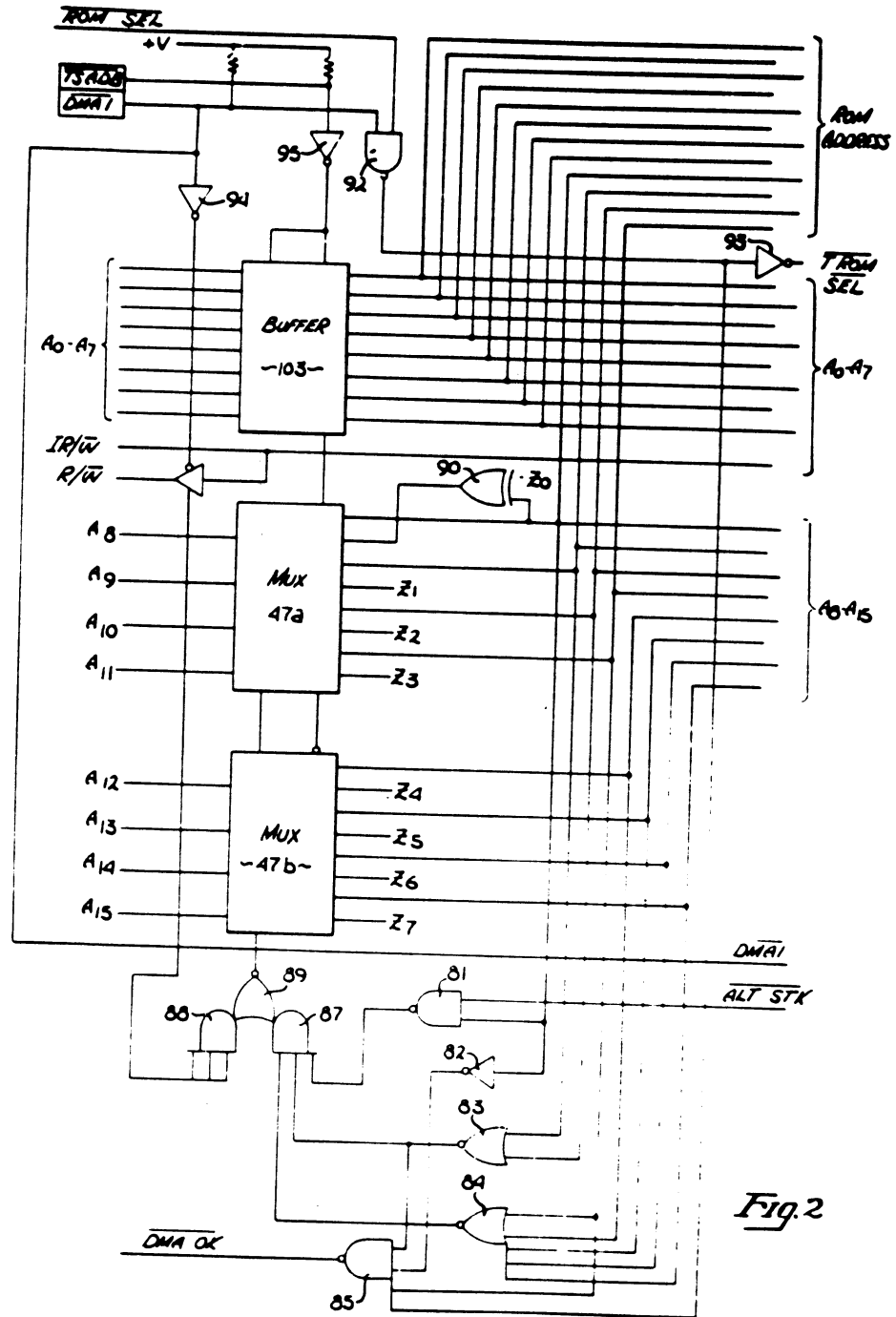


Fig. 2

Source III PATENT—AUG 1985

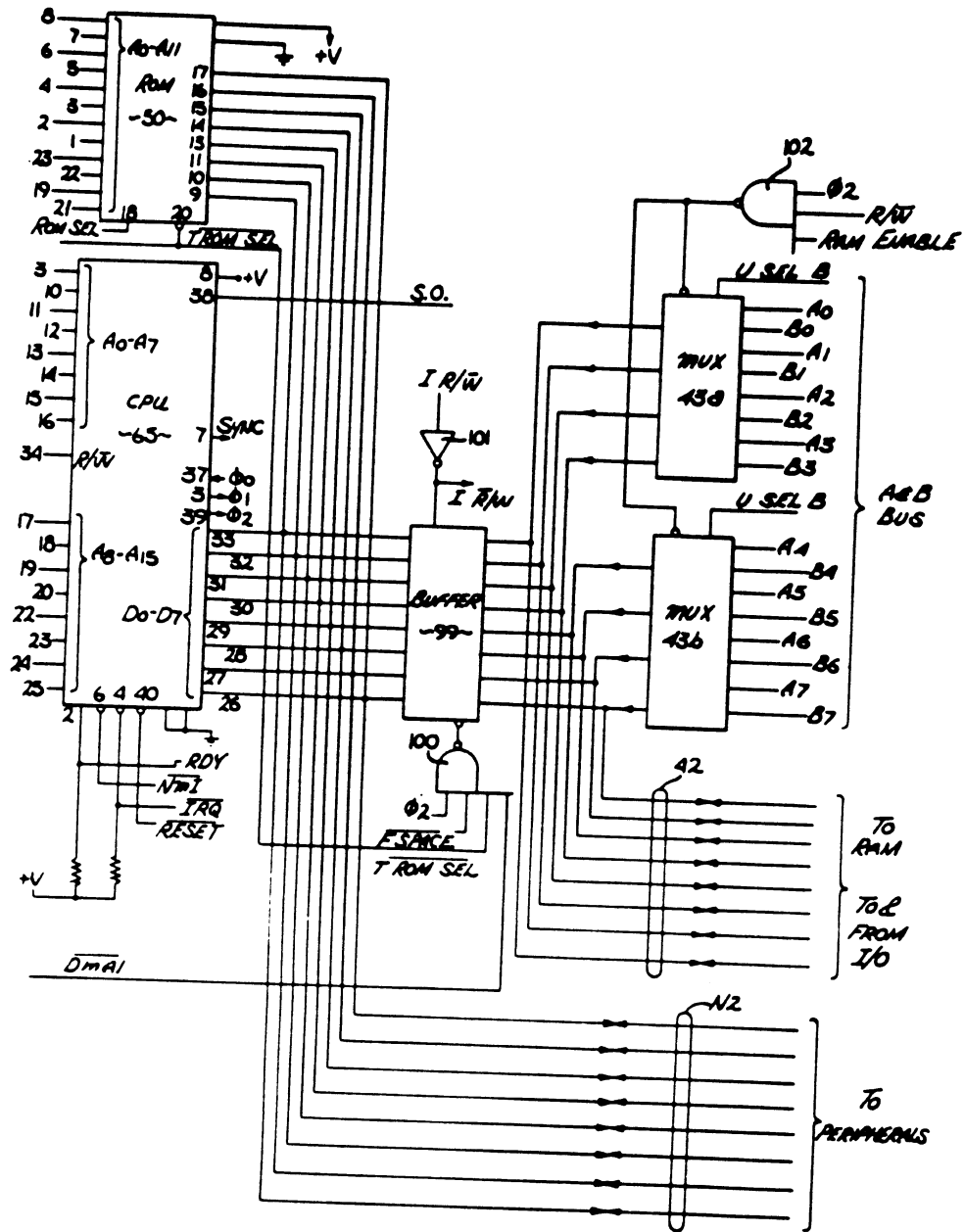


Fig. 3

Source III PATENT—AUG 1985

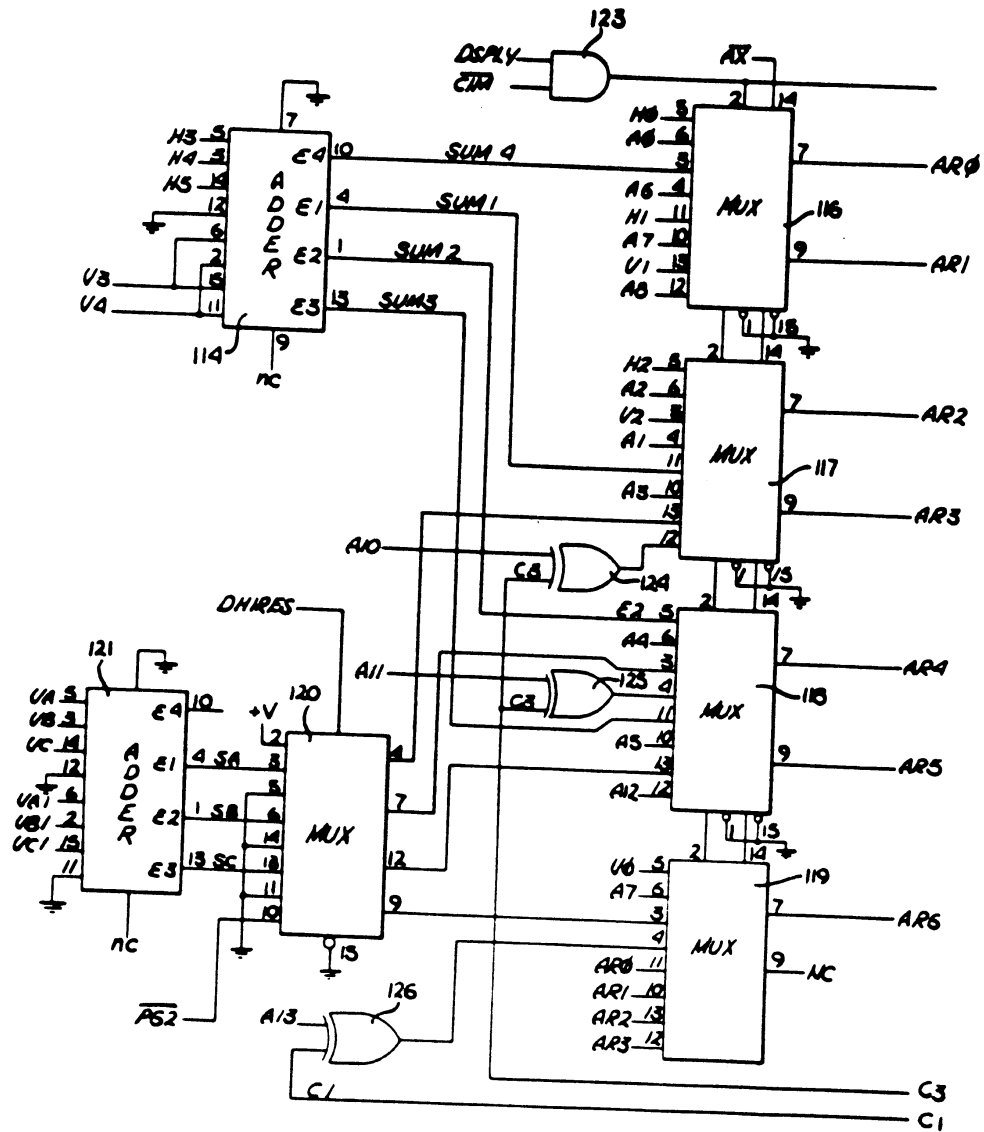
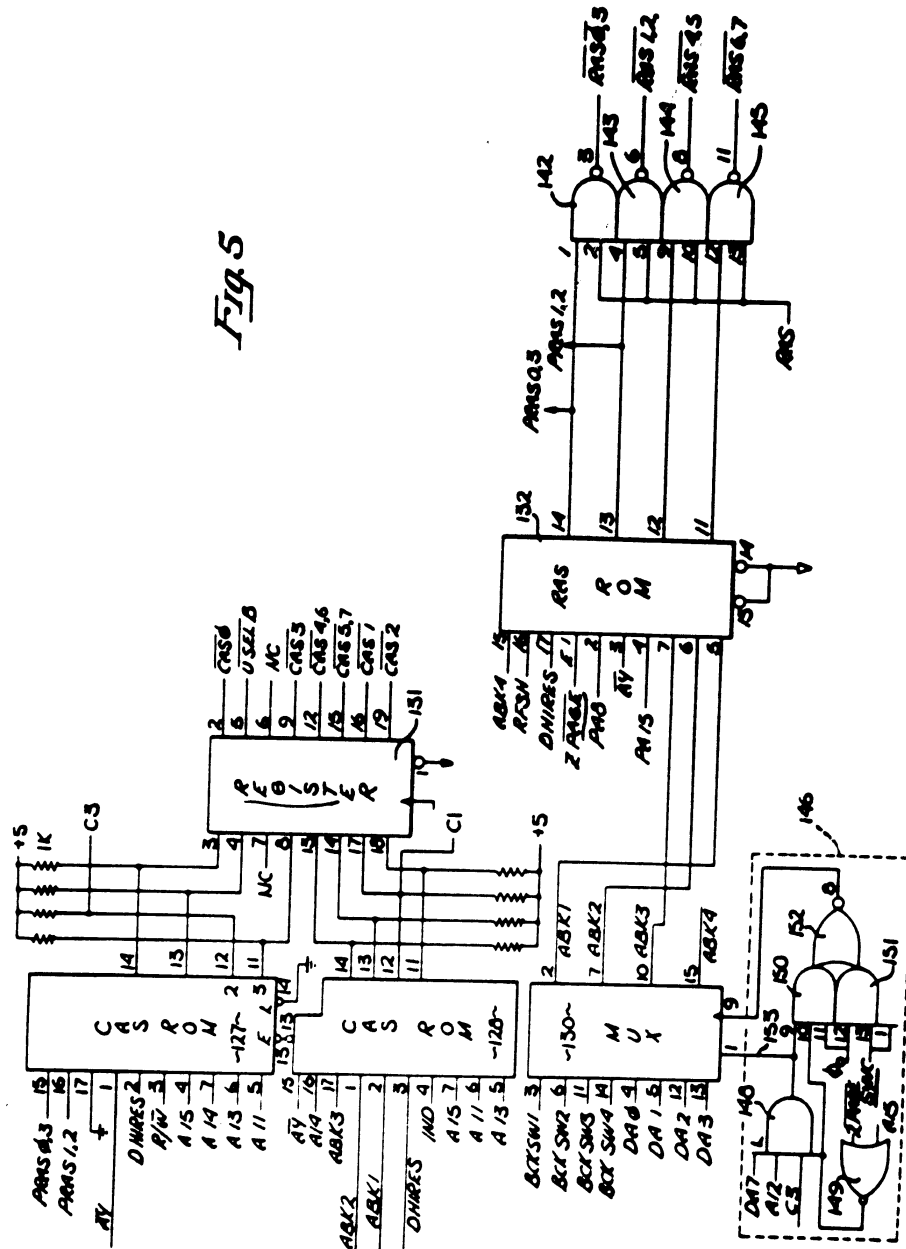


Fig. 4

Source /// PATENT - AUG 1985



Source */// PATENT - AUG 1985*

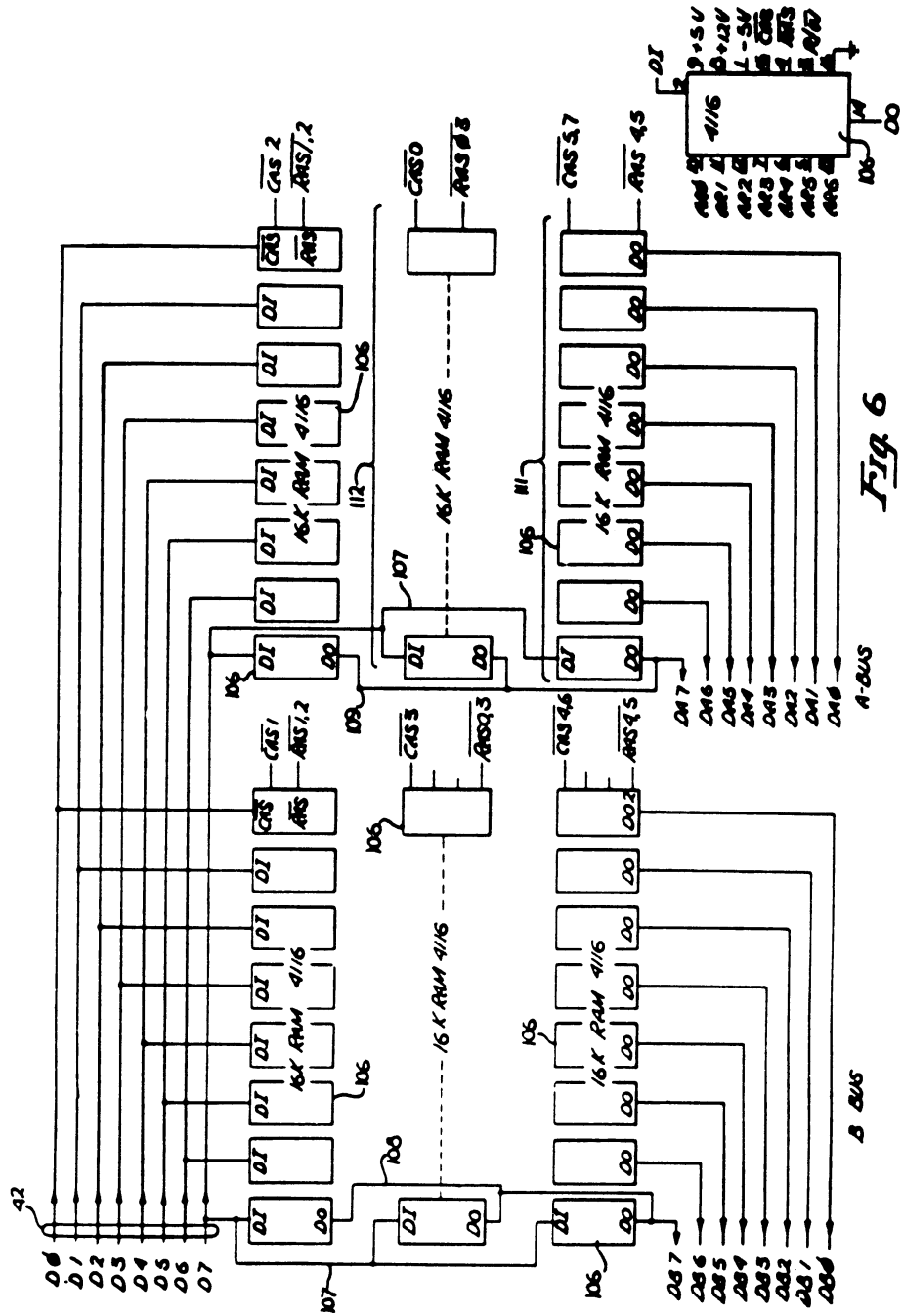


Fig. 6

Source III PATENT — AUG 1985

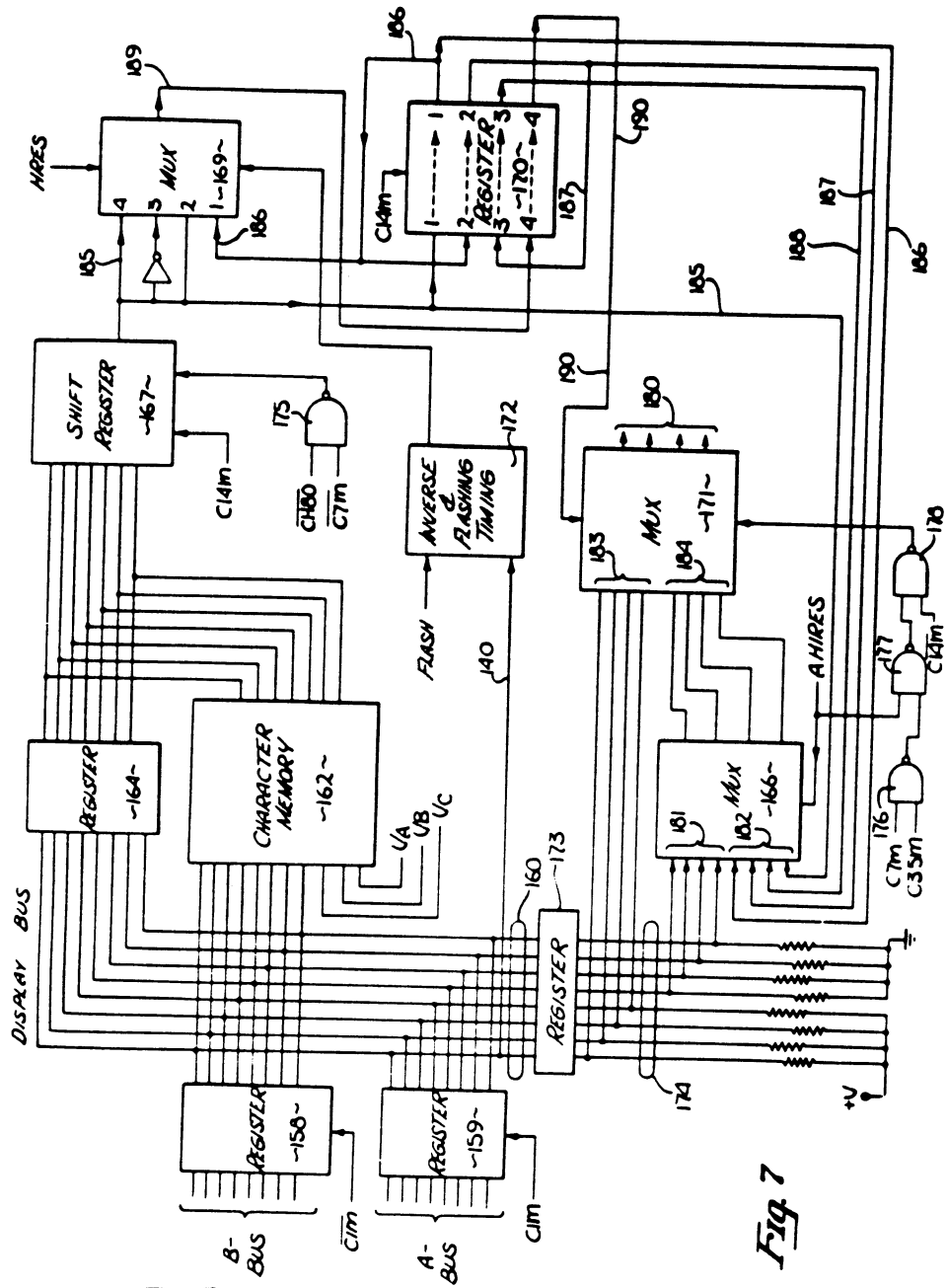


Fig. 7

Source /// PATENT - AUG 1985

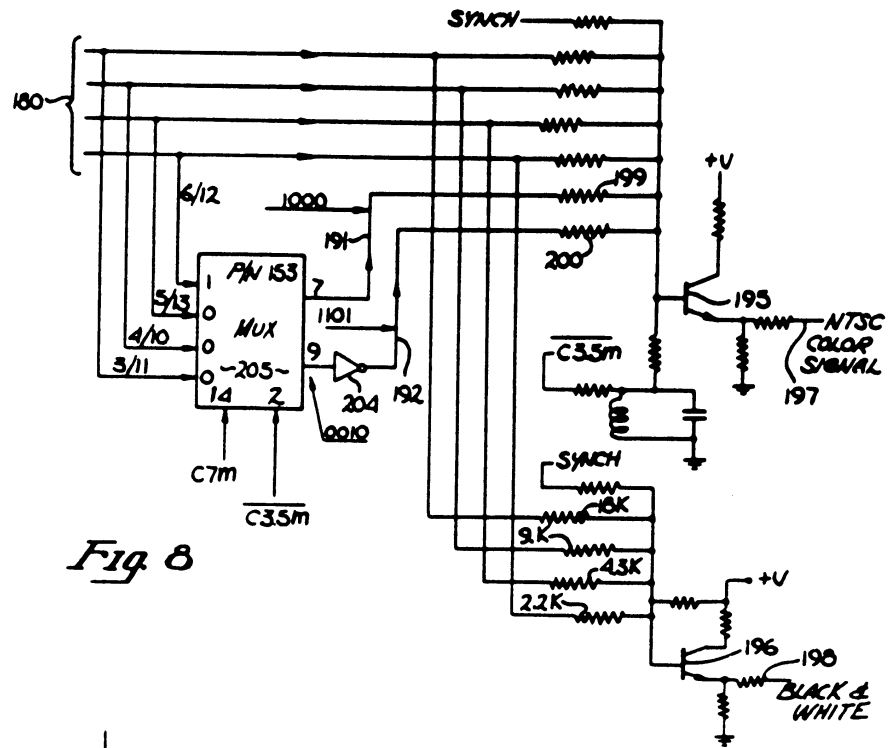


Fig 8

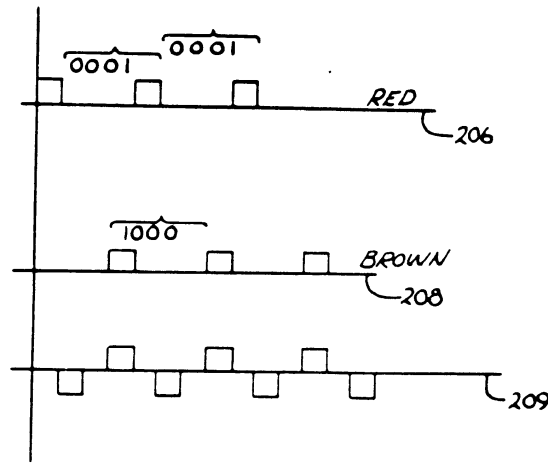


Fig 9

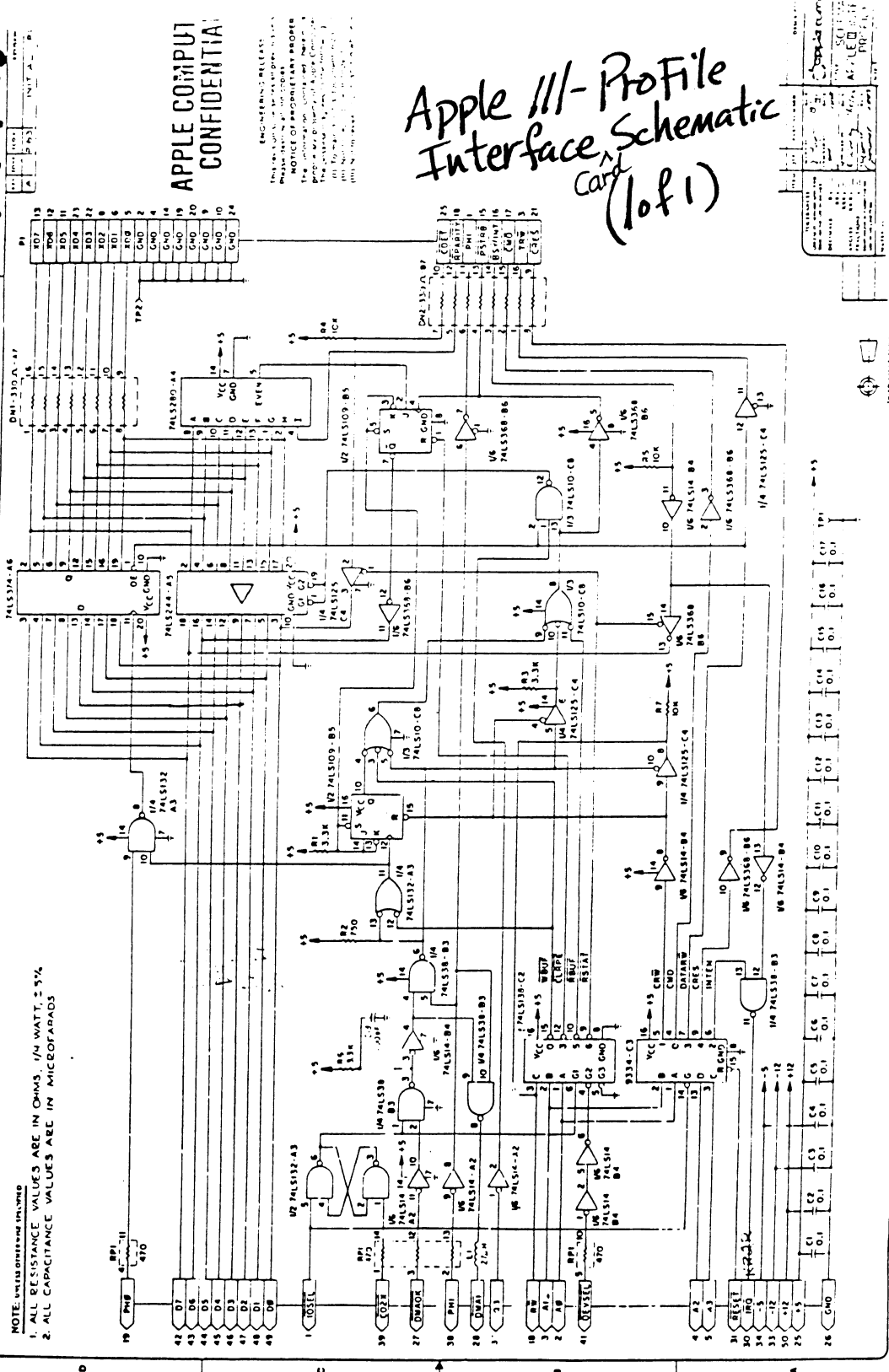
Source /// PATENT - AUG 1985

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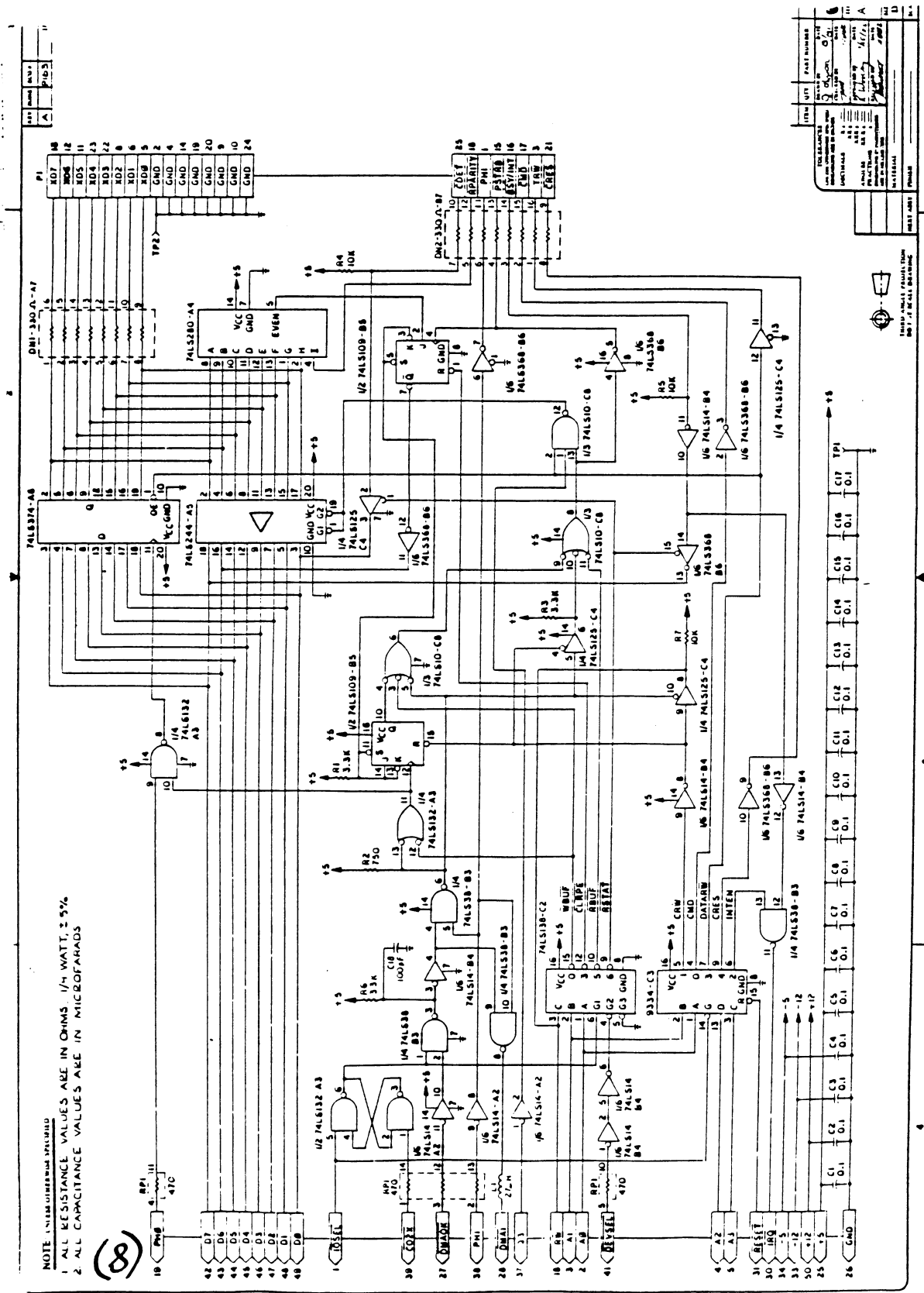
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Apple ///-Profile
Interface Schematic
Card (of 1)

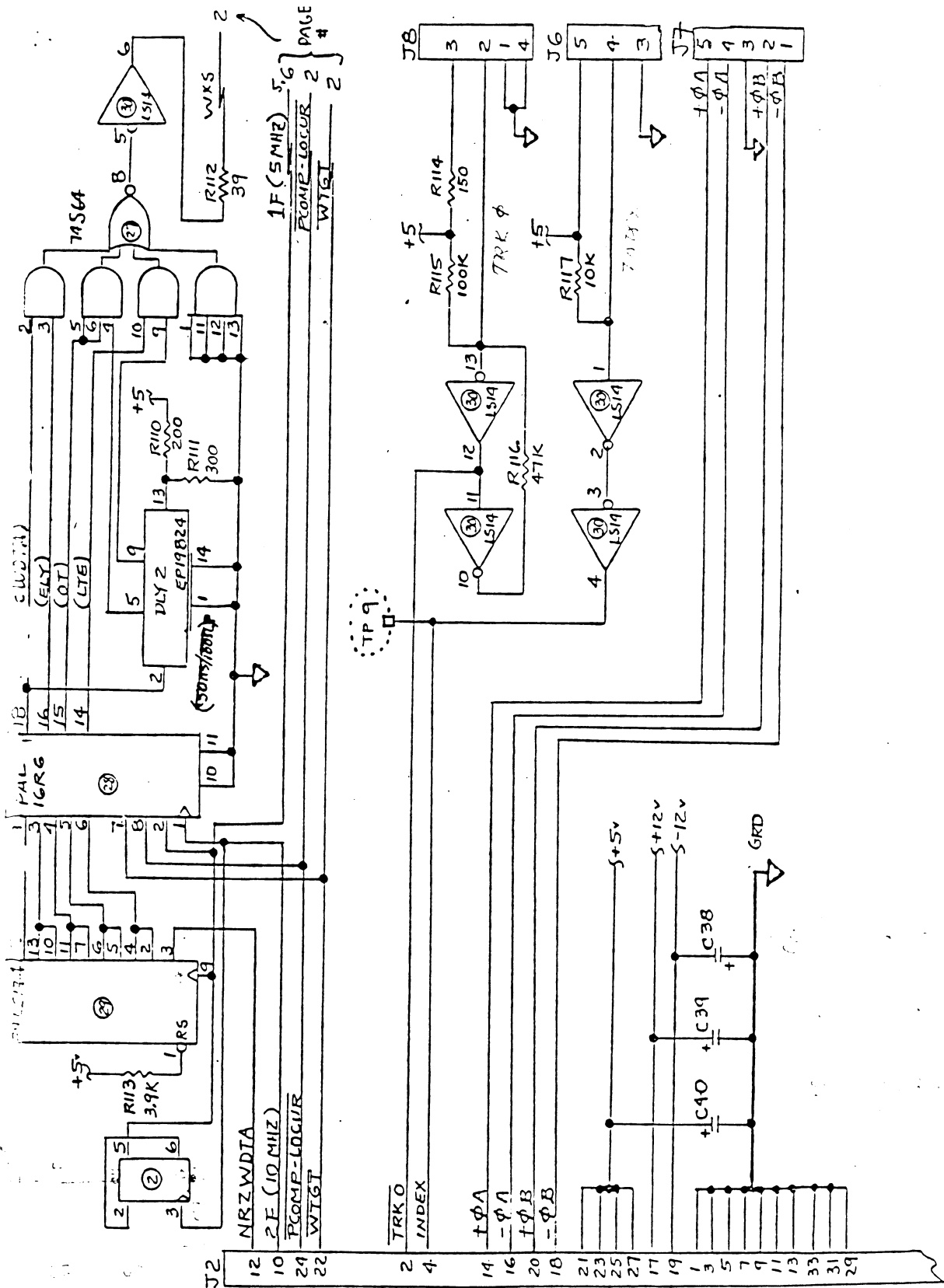


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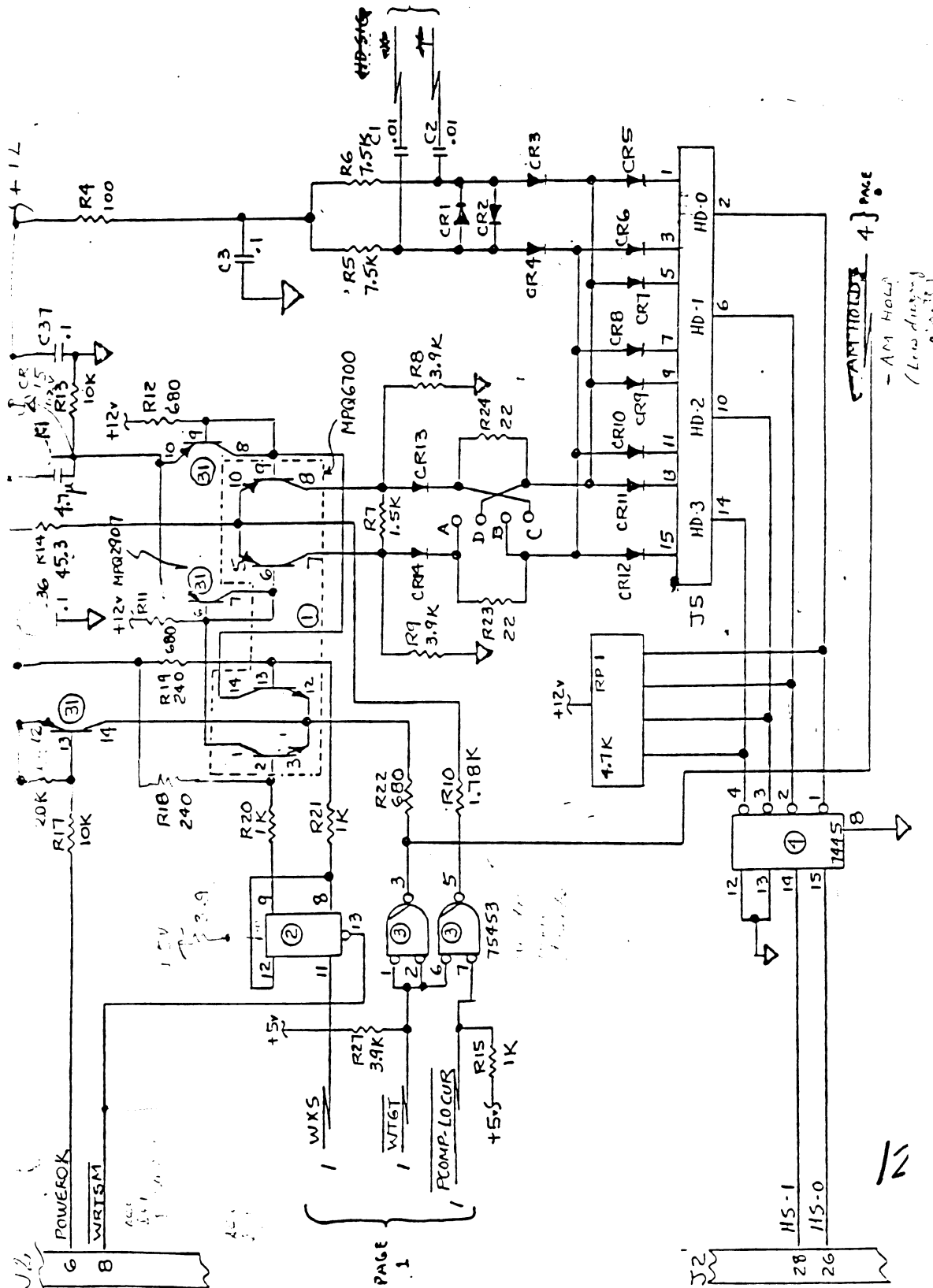
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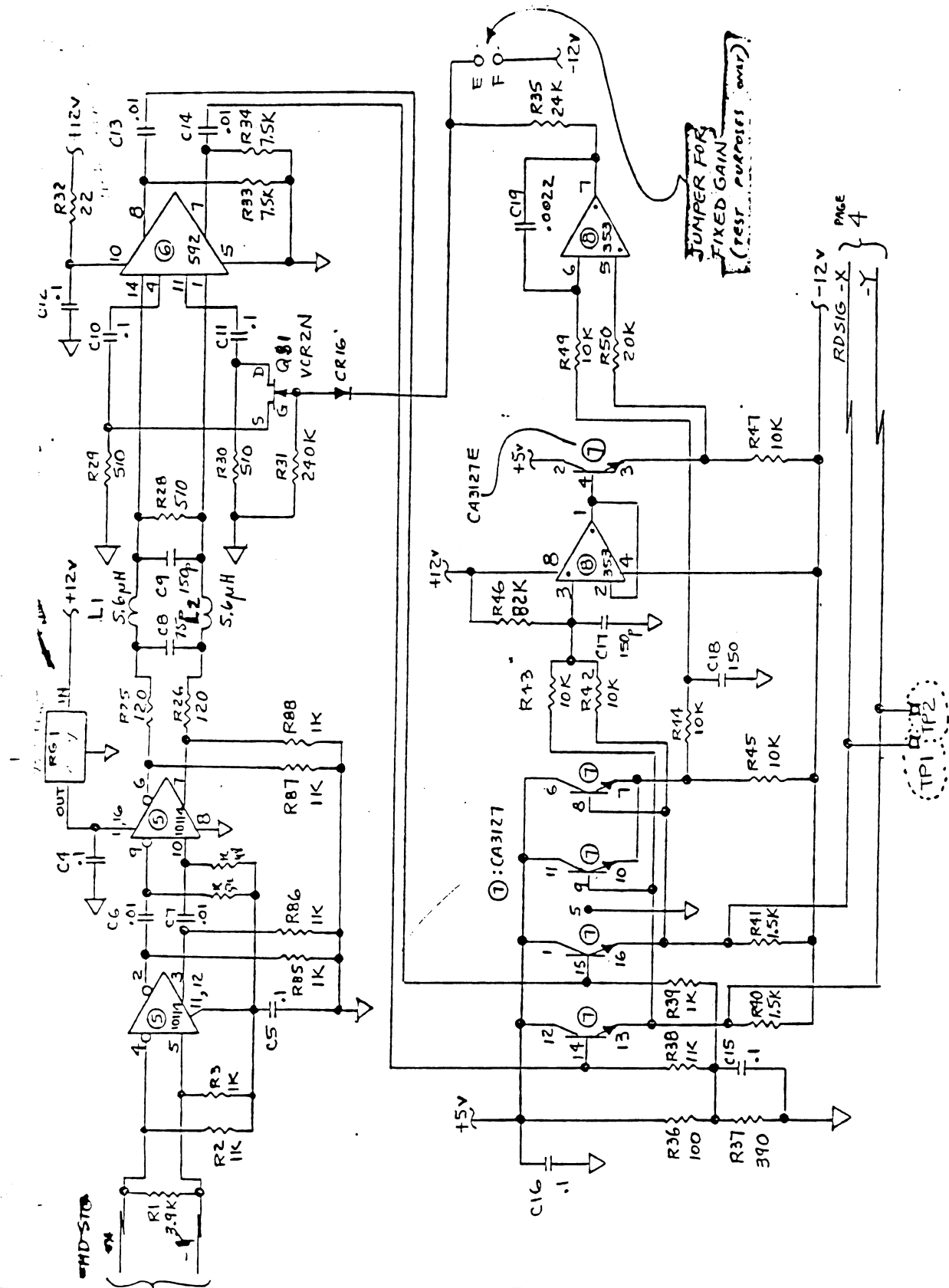
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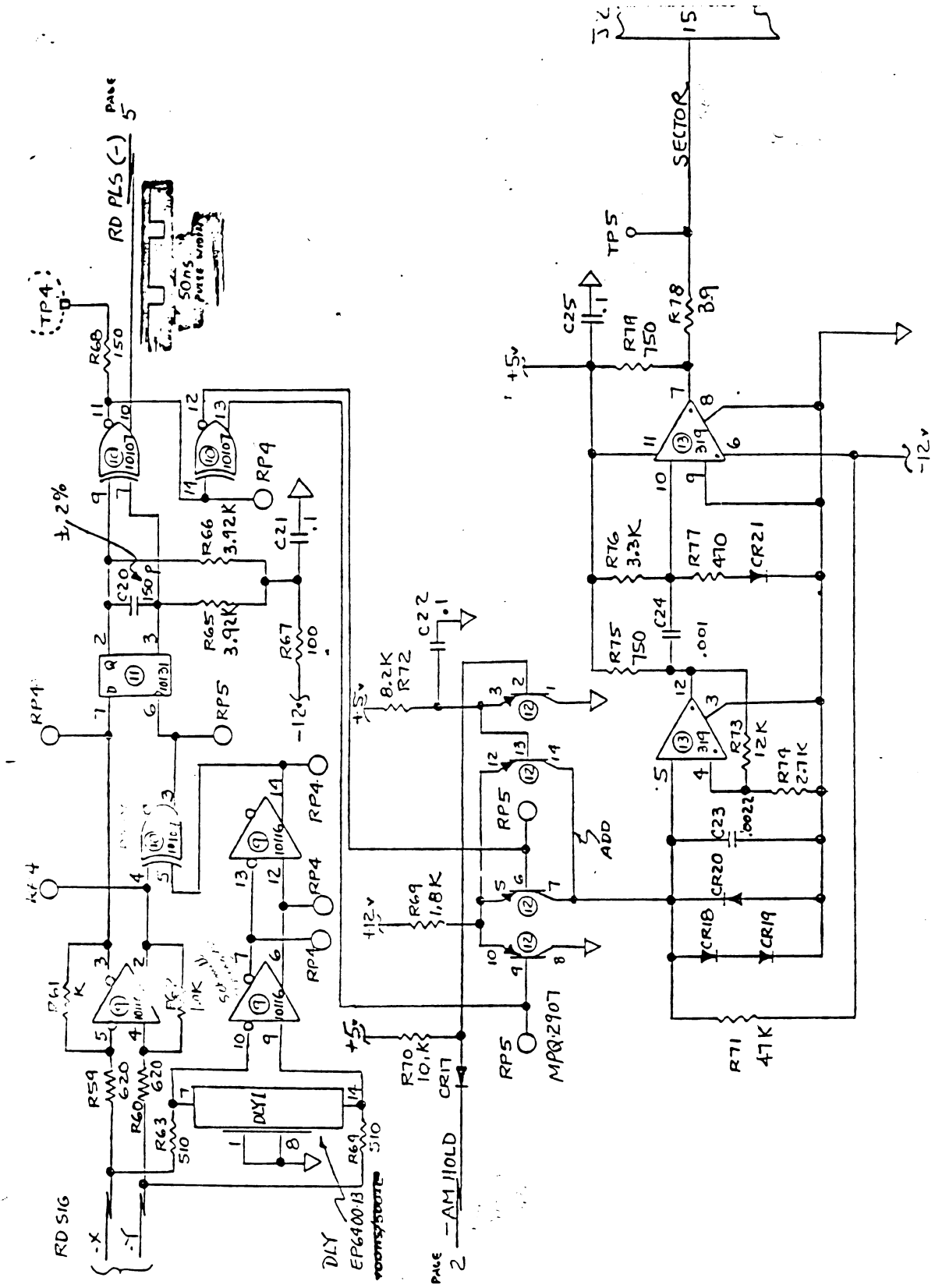
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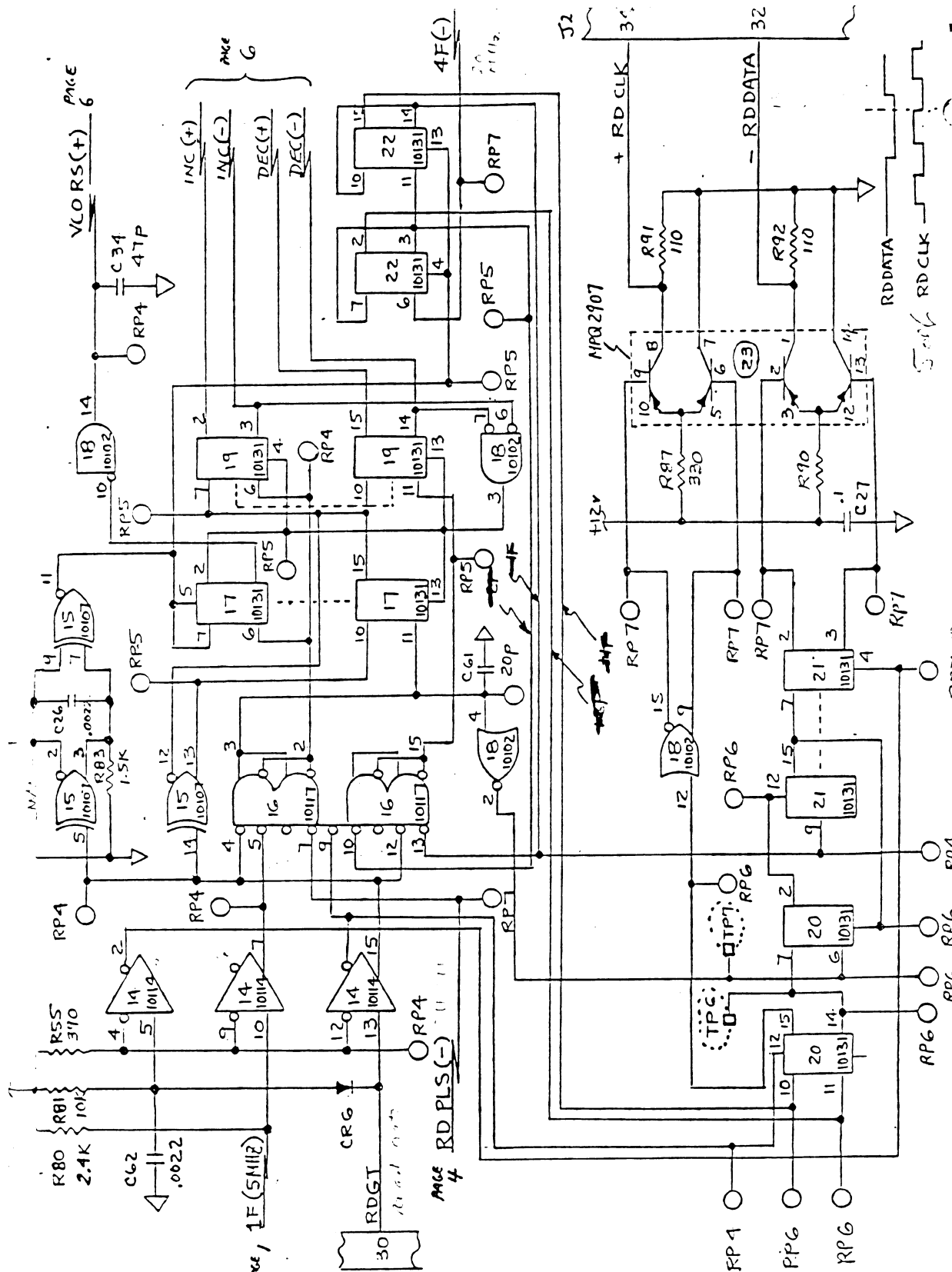
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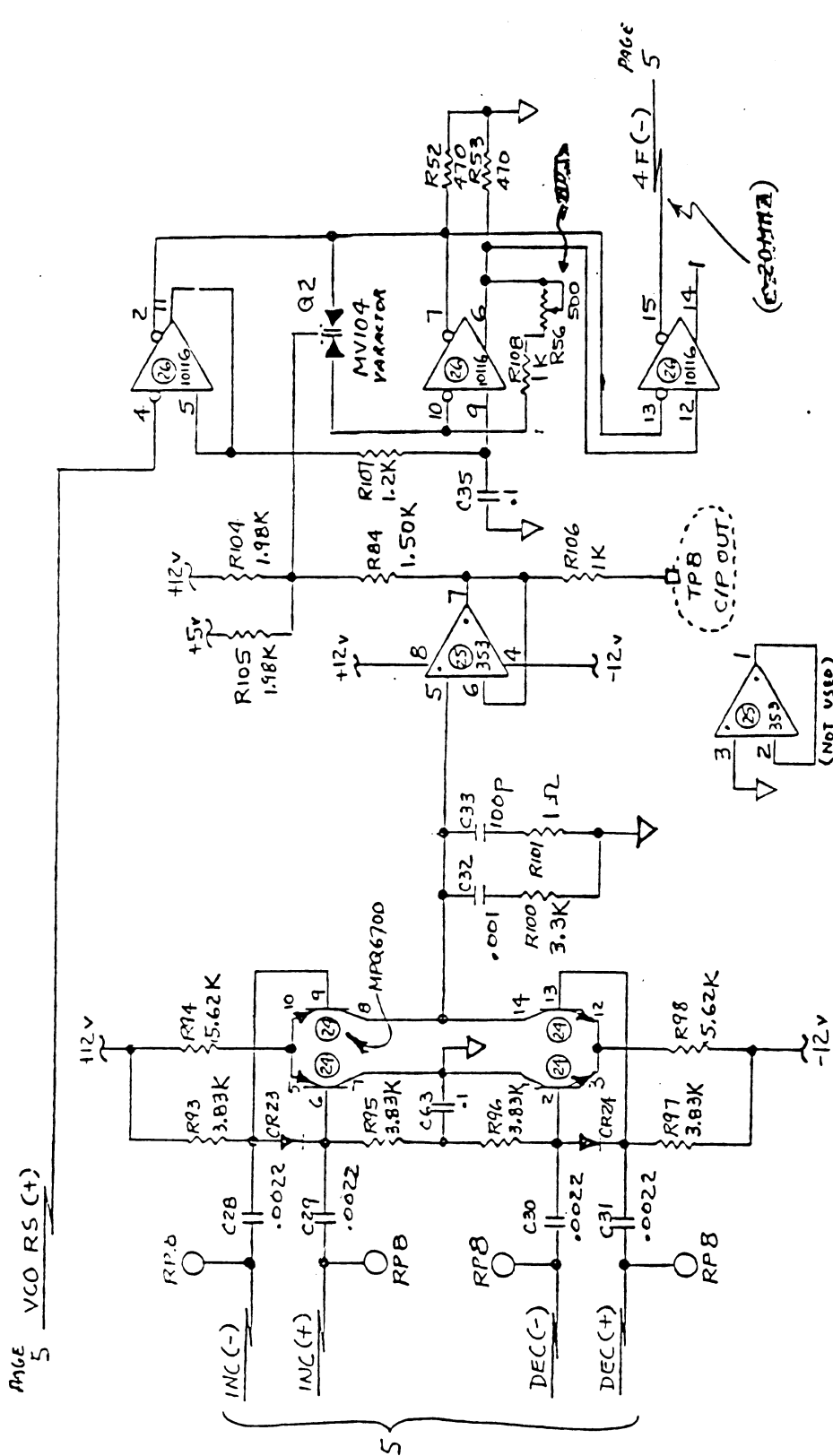
Source PROFILE SERVICE



Source PROFILE SERVICE



Source PROFILE SERVICE



REV DATE : 5/5/81
 0P3

Source PROFILE SERVICE



Apple /// Computer Schematics

Source
Apple Service
Level II Technical Reference
204-1022
Volume II

SCHEMATIC LIST

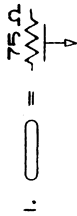
Disk Analog	050-0031-00	05/1980
Disk Analog	050-0031-C	04/1981
Main Memory Board	050-0032-E	05/1980
Main Logic # 2	050-0039-H	06/1982
Parallel Printer Card	050-0042-A	04/1982
5V Memory Board	050-0044-B	05/1981
ProFile Analog Board	050-5005-B	01/1982
ProFile Controller Board	050-5006-A	01/1982
ProFile Apple /// Interface Card	050-5007-A	01/1982

Compiled by

David T Craig

April 2003

NOTE: UNLESS OTHERWISE SPECIFIED



2. \square = ALL UNITS UNDER TEST MOLEX PINS TO BE LOCATED TOGETHER.

3. \circ = ALL TIMING MOLEX PINS TO BE LOCATED TOGETHER.

4. THIS SCHEMATIC REPRESENTS ASSY 610-0105 AT REV LEVEL: F.

FOR STANDARD SYSTEMS G9 IS 341-0030, FOR EURO SYSTEMS G9 IS 341-0060.

FOR STANDARD SYSTEMS Y1 IS 14.318630 MHZ, FOR EURO SYSTEMS Y1 IS 14.250450 MHZ.

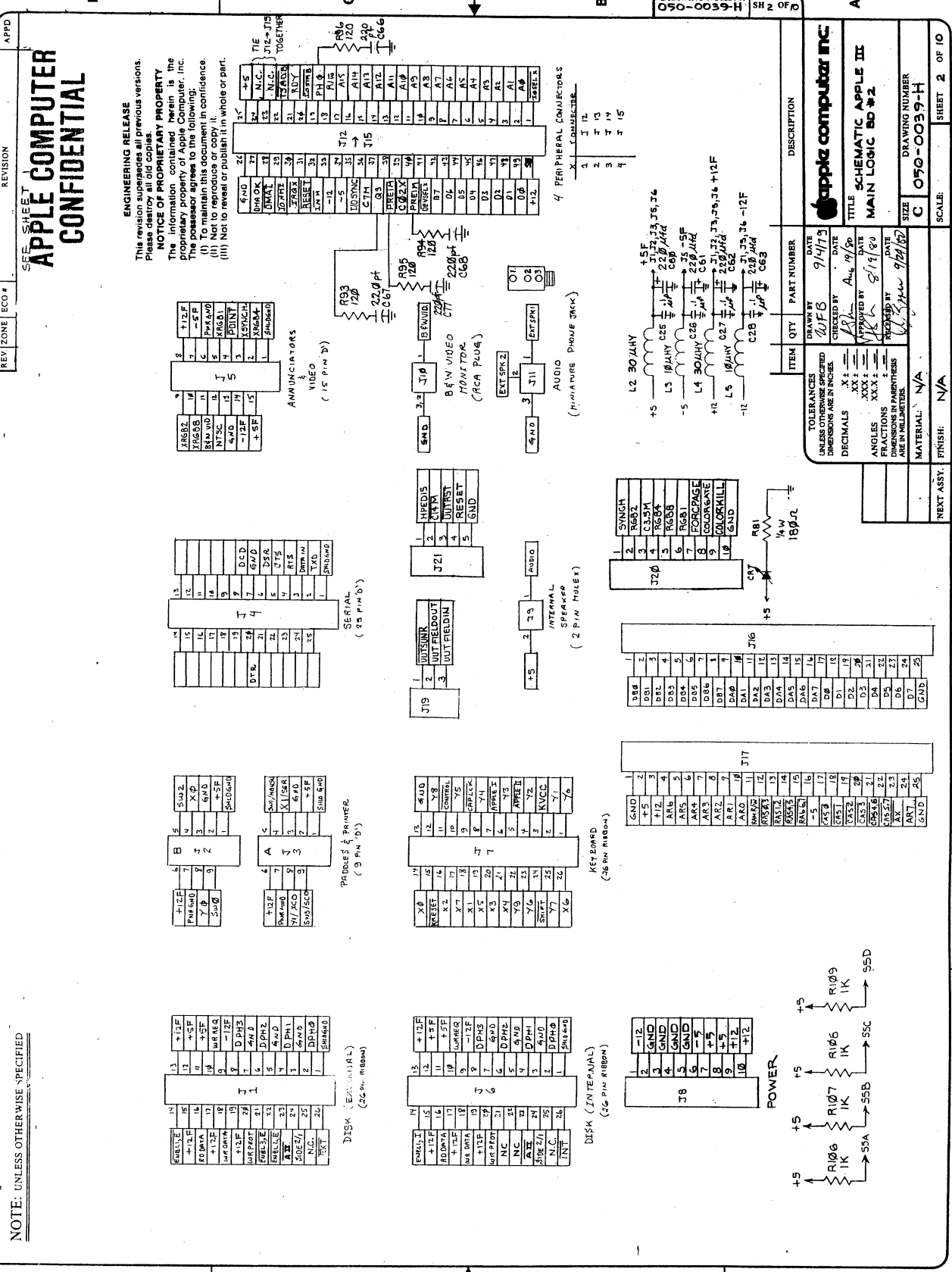
REV	ZONE	ECO #	REVISION	APPD
O2			ENG. RELEASE	
O3			PRE-PRODUCTION RELEASE	
E			PRE-PRODUCTION CHANGES	
E		504	ECO RELEASE	
E		544	DELETED CAP ARRAY (CBI), AND N15, N13, K13, N3, N10 WAS PC NETWORK, C5 WAS H7PF, G1 WAS G6, N, C, I, IS NOW 10STOPD, J20, 7 WAS COLORKILL, J20, 9 WAS FORPAGE, DELETED MICROPROCESSOR (B3)	
G		778	H8 WAS L504, R15 WAS L7 OHM, R16 WAS 75 OHM, ADDED 1K OHM RESISTOR AT K10.	
H		923	CHANGE CAP C22 FROM 1 uF TO .022 uF, CHANGE RP-4.	

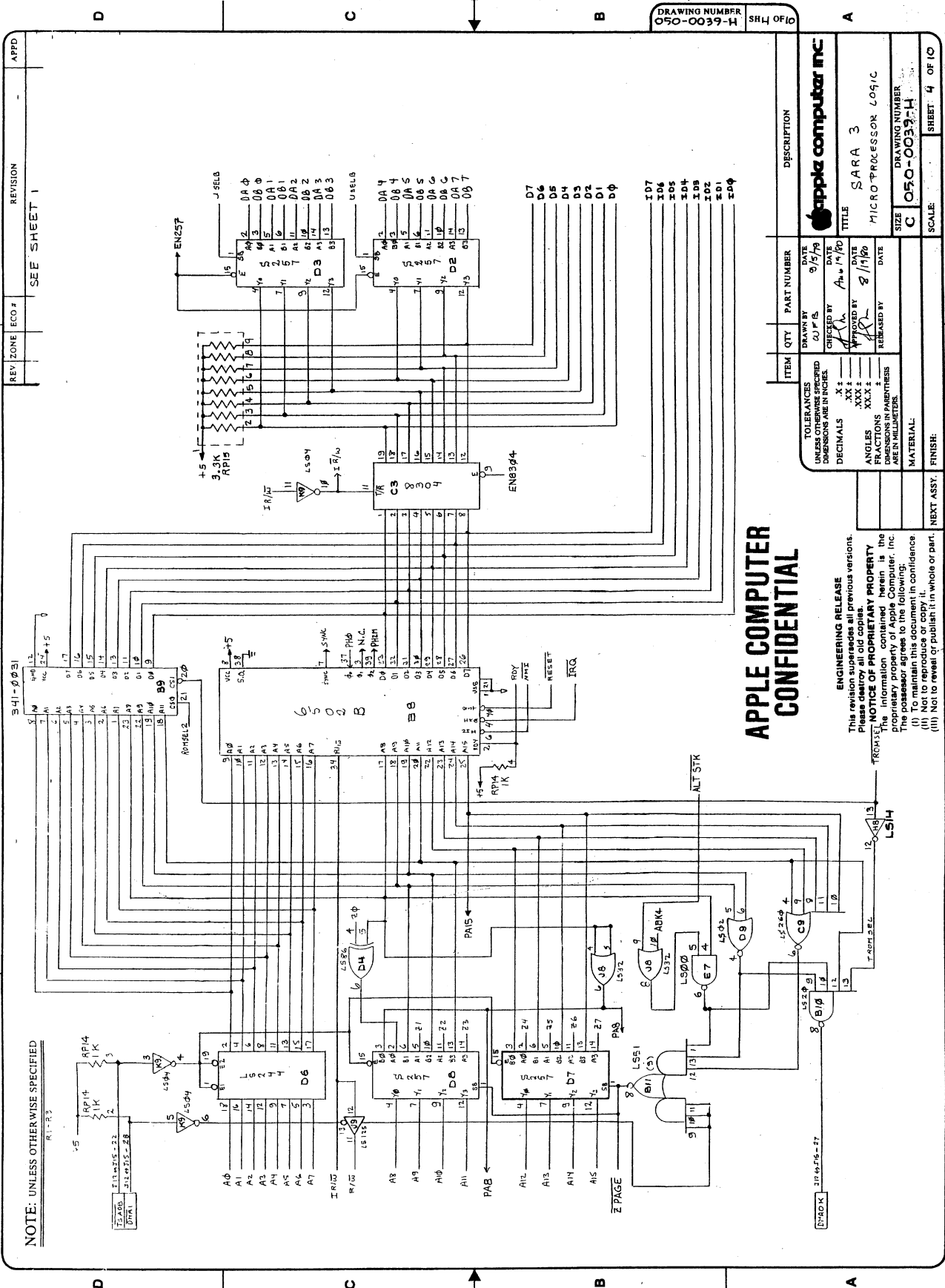
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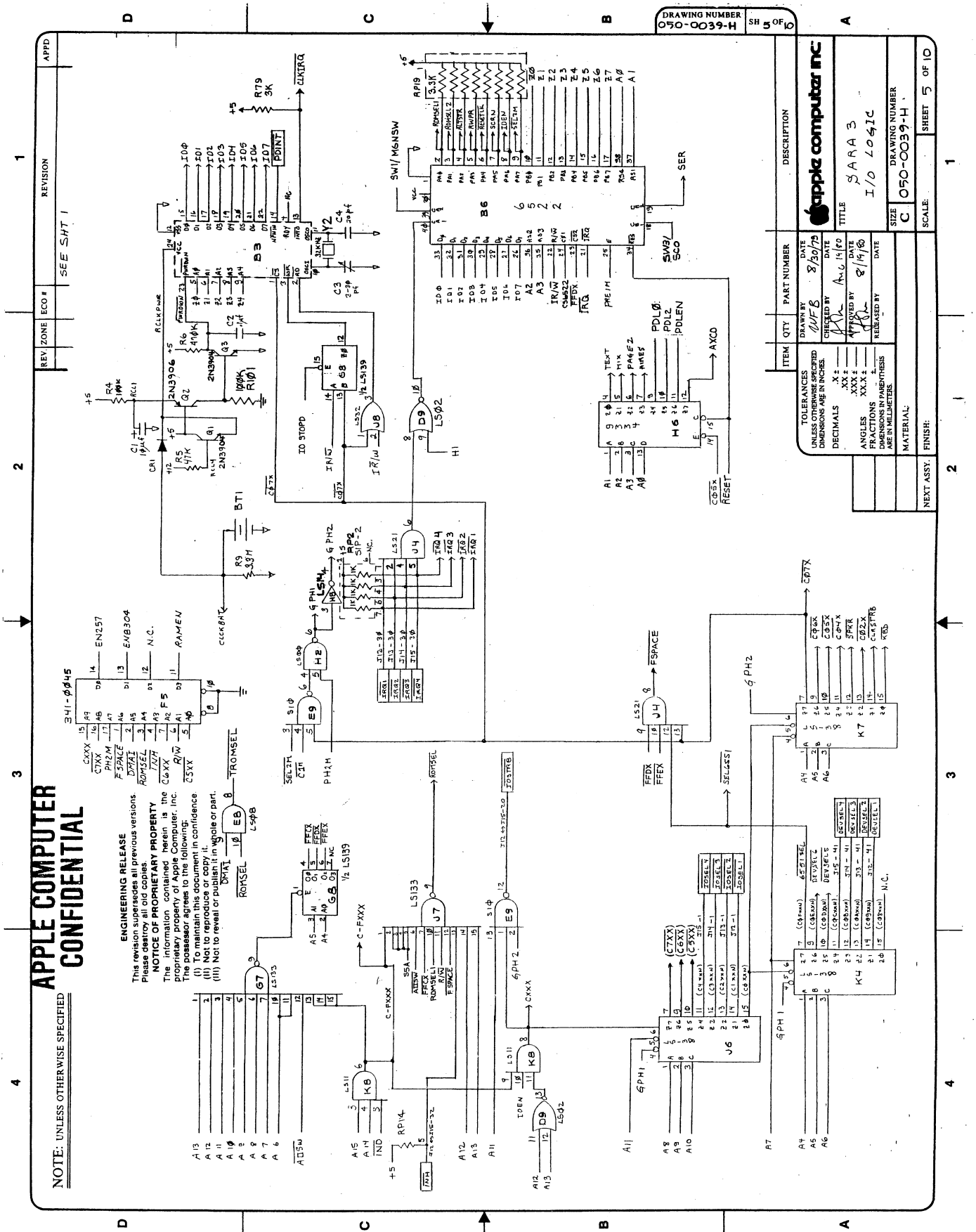
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DRAWING NUMBER
050-0039-H SH1 OF 10

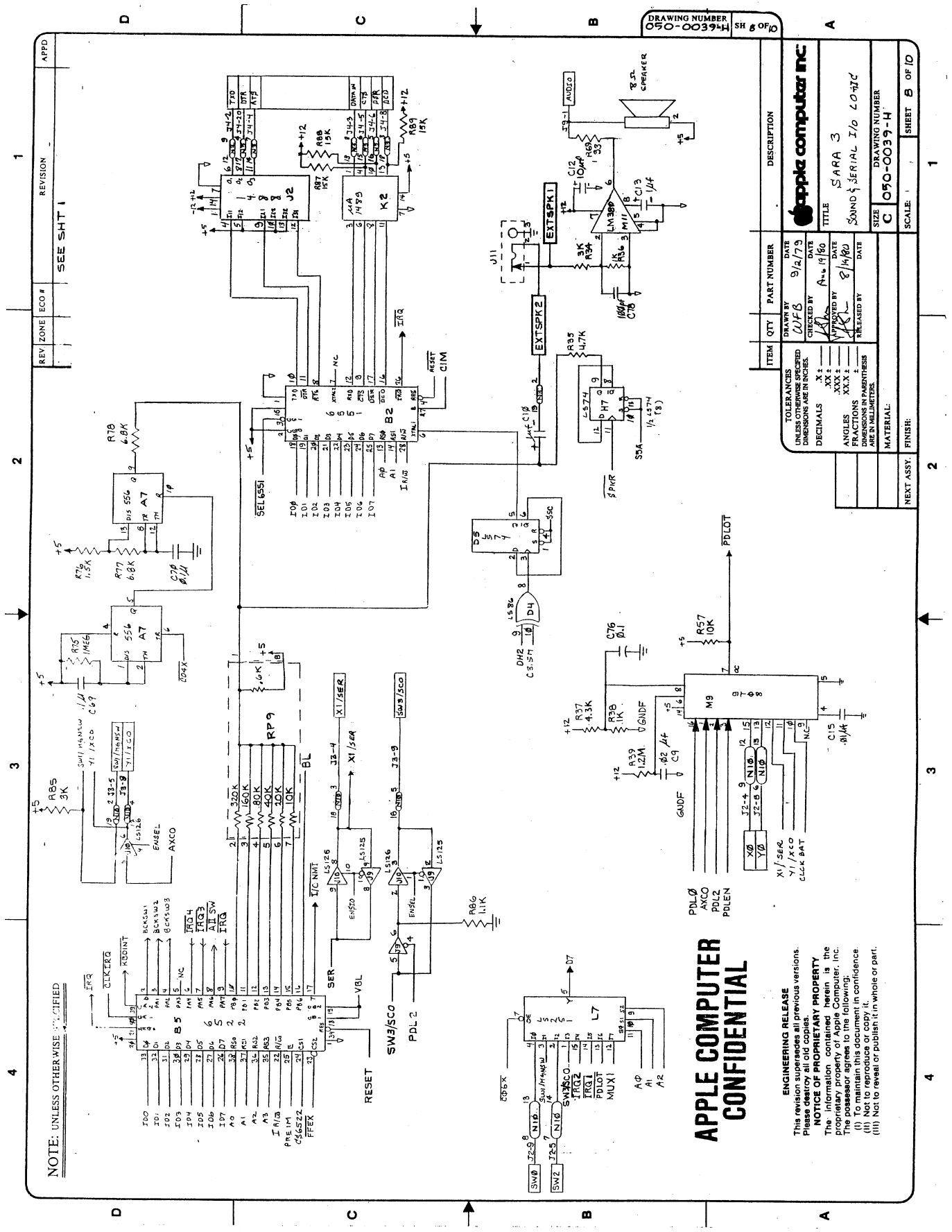
ITEM	QTY	PART NUMBER	DESCRIPTION																																
<table border="0"> <tr> <td>TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES</td> <td>DRAWN BY</td> <td>DATE</td> <td></td> </tr> <tr> <td>DECIMALS .X ±</td> <td>WFB</td> <td>9-4-79</td> <td></td> </tr> <tr> <td>ANGLES .XX ±</td> <td>CHECKED BY</td> <td>DATE</td> <td></td> </tr> <tr> <td>FRACTIONS .XXX ±</td> <td>JMcDonald</td> <td>8-19-80</td> <td></td> </tr> <tr> <td>DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS</td> <td>APPROVED BY</td> <td>DATE</td> <td></td> </tr> <tr> <td></td> <td>JMcDonald</td> <td>8-19-80</td> <td></td> </tr> <tr> <td>MATERIAL: N/A</td> <td>RELEASED BY</td> <td>DATE</td> <td></td> </tr> <tr> <td></td> <td>JMcDonald</td> <td>8-28-80</td> <td></td> </tr> </table>				TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DRAWN BY	DATE		DECIMALS .X ±	WFB	9-4-79		ANGLES .XX ±	CHECKED BY	DATE		FRACTIONS .XXX ±	JMcDonald	8-19-80		DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS	APPROVED BY	DATE			JMcDonald	8-19-80		MATERIAL: N/A	RELEASED BY	DATE			JMcDonald	8-28-80	
TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DRAWN BY	DATE																																	
DECIMALS .X ±	WFB	9-4-79																																	
ANGLES .XX ±	CHECKED BY	DATE																																	
FRACTIONS .XXX ±	JMcDonald	8-19-80																																	
DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS	APPROVED BY	DATE																																	
	JMcDonald	8-19-80																																	
MATERIAL: N/A	RELEASED BY	DATE																																	
	JMcDonald	8-28-80																																	
			TITLE SCHEMATIC APPLE /// MAIN LOGIC #2																																
NEXT ASSY: FINISH: N/A			SIZE 050-0039-H																																
DRAWING NUMBER			SHEET 1 OF 10																																







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ITEM	QTY	PART NUMBER	DESCRIPTION
DRAWN BY: UJFB DATE: 9/2/79			
CHECKED BY: A.L. DATE: 10/1/80			
APPROVED BY: [Signature] DATE: 8/14/80			
RELEASED BY: [Signature] DATE: [Blank]			
DRAWING NUMBER: C 1050-0039-H			
TITLE: SARA 3 SERIAL I/O CONTROLLER			
DRAWING NUMBER: C 1050-0039-H			
SHEET: 1 OF 1			

REV	ZONE	ECO #	REVISION
1			SEE SHT 1

APPD

REV

APPD

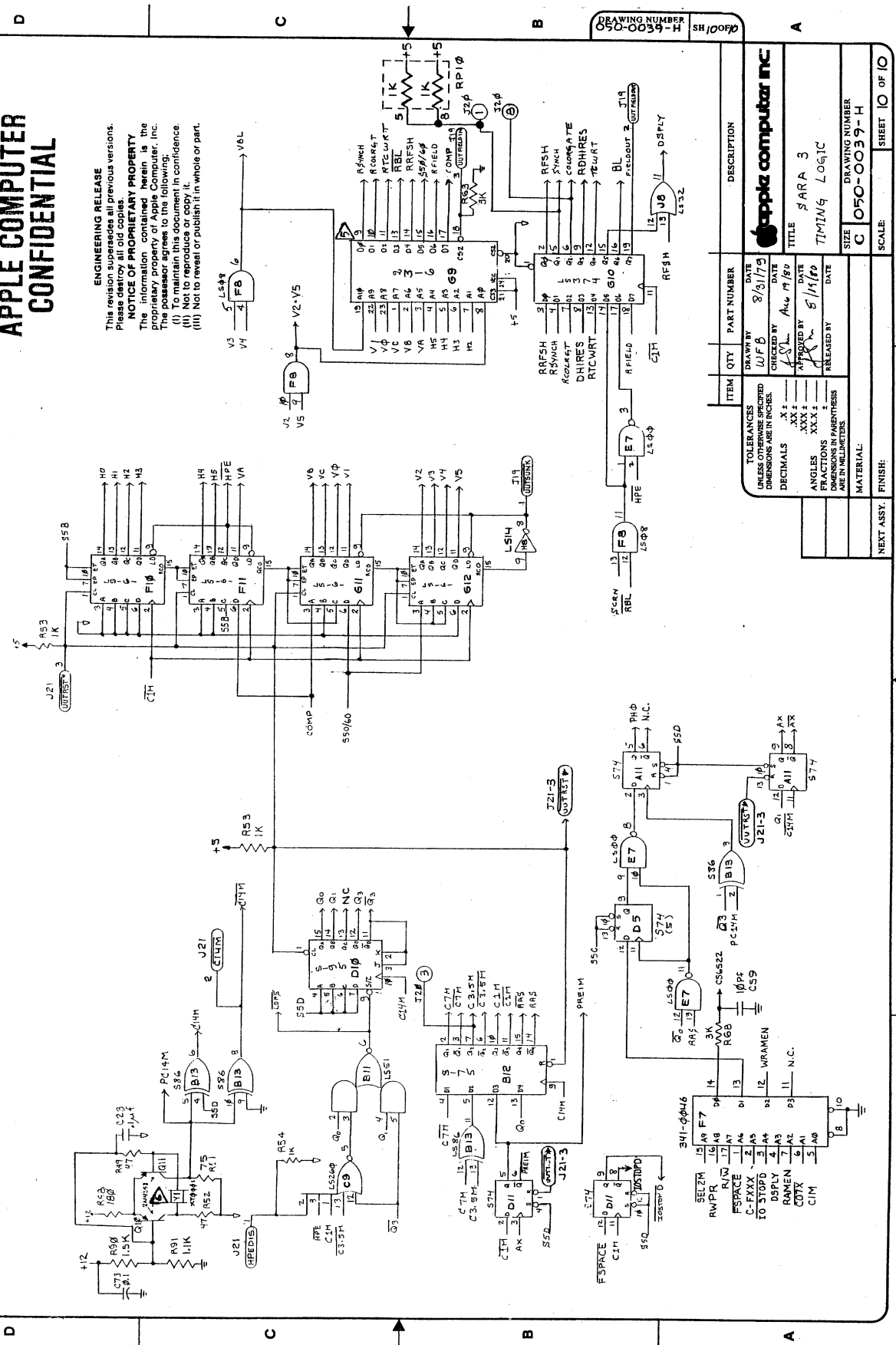
REV

APPD

REV. ZONE	ECO #	REVISION
		SEE SHT 1

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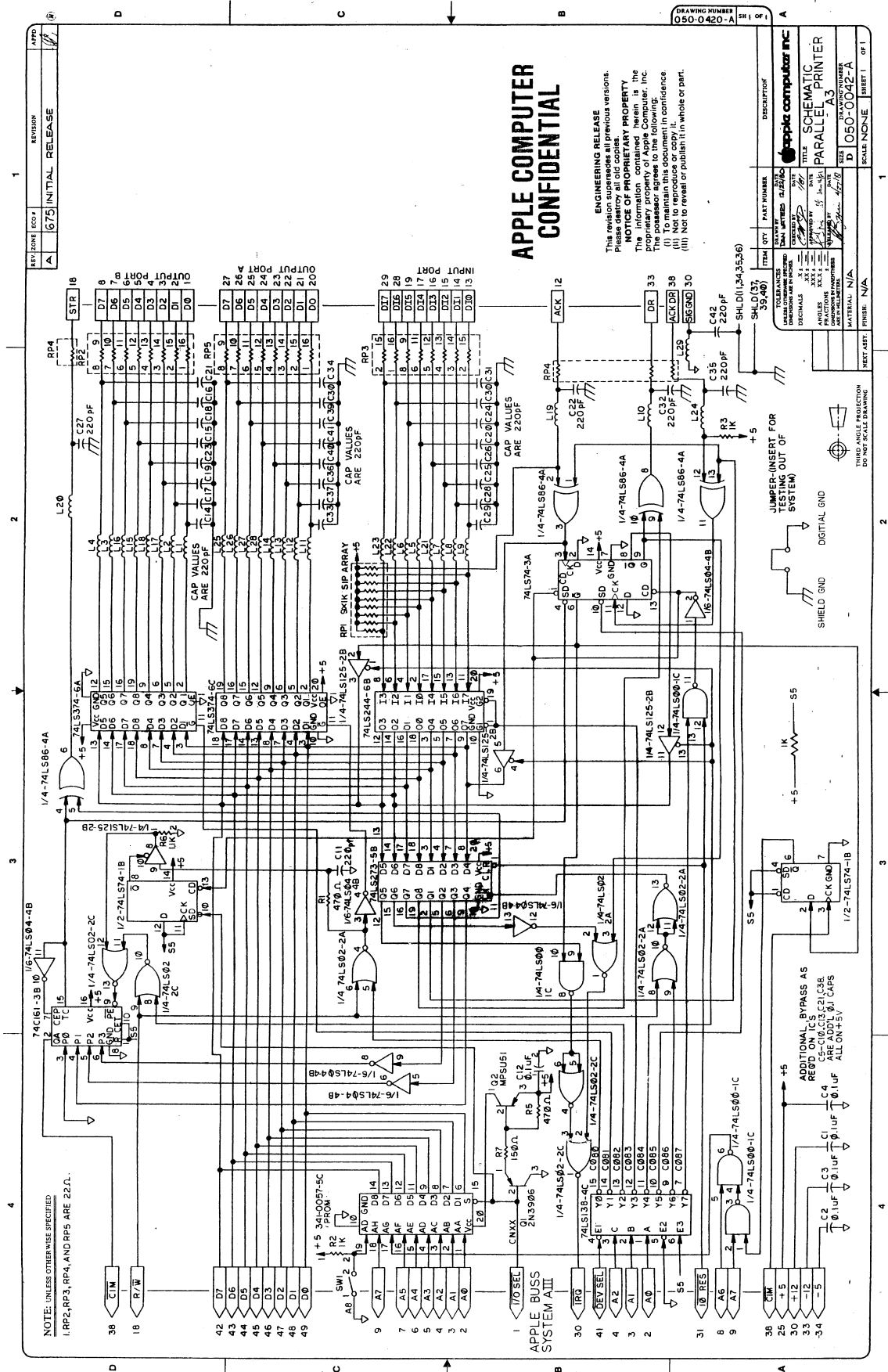
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DRAWING NUMBER
050-0039-H

DRAWING NUMBER 050-0039-H		SH/00FP	
DRAWN BY WFB		DATE 8/31/79	
CHECKED BY AWM		DATE 9/17/80	
APPROVED BY RJA		DATE 5/11/80	
RELEASED BY		DATE	
TOLERANCES UNLESS OTHERWISE SPECIFIED		DESCRIPTION	
DIMENSIONS ARE IN INCHES		ITEM	
DECIMALS .XX		QTY	
FRACTIONS XX/XX		PART NUMBER	
ANGLES XX.X		DRAWN BY	
DIMENSIONS IN PARENTHESES ARE ENVELOPES		DATE	
MATERIAL:		DRAWING NUMBER	
NEXT ASSY:		SCALE:	
FINISH:		SHEET 10 OF 10	

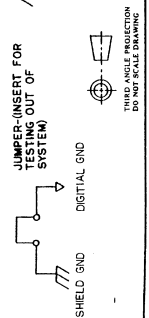


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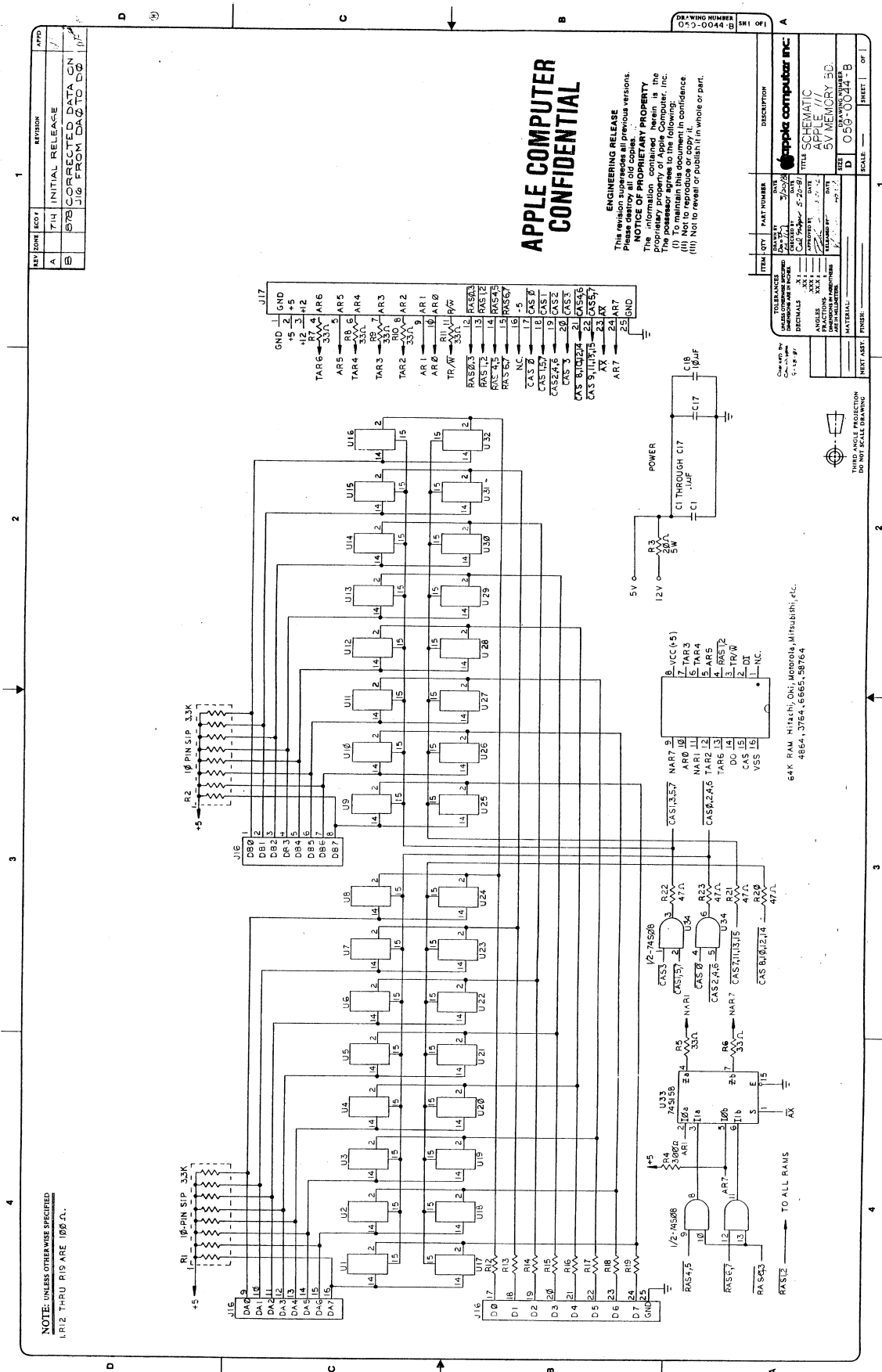
DRAWING NUMBER	SR 1 OF 1
050-0420-A	
DESCRIPTION	SCHEMATIC PARALLEL A3
DATE	10/18/82
DESIGNED BY	W. J. ...
CHECKED BY	...
APPROVED BY	...
SCALE	NONE
SHEET	001

NOTE: UNLESS OTHERWISE SPECIFIED
1. RP2, RP3, RP4, AND RP5 ARE 22Ω.



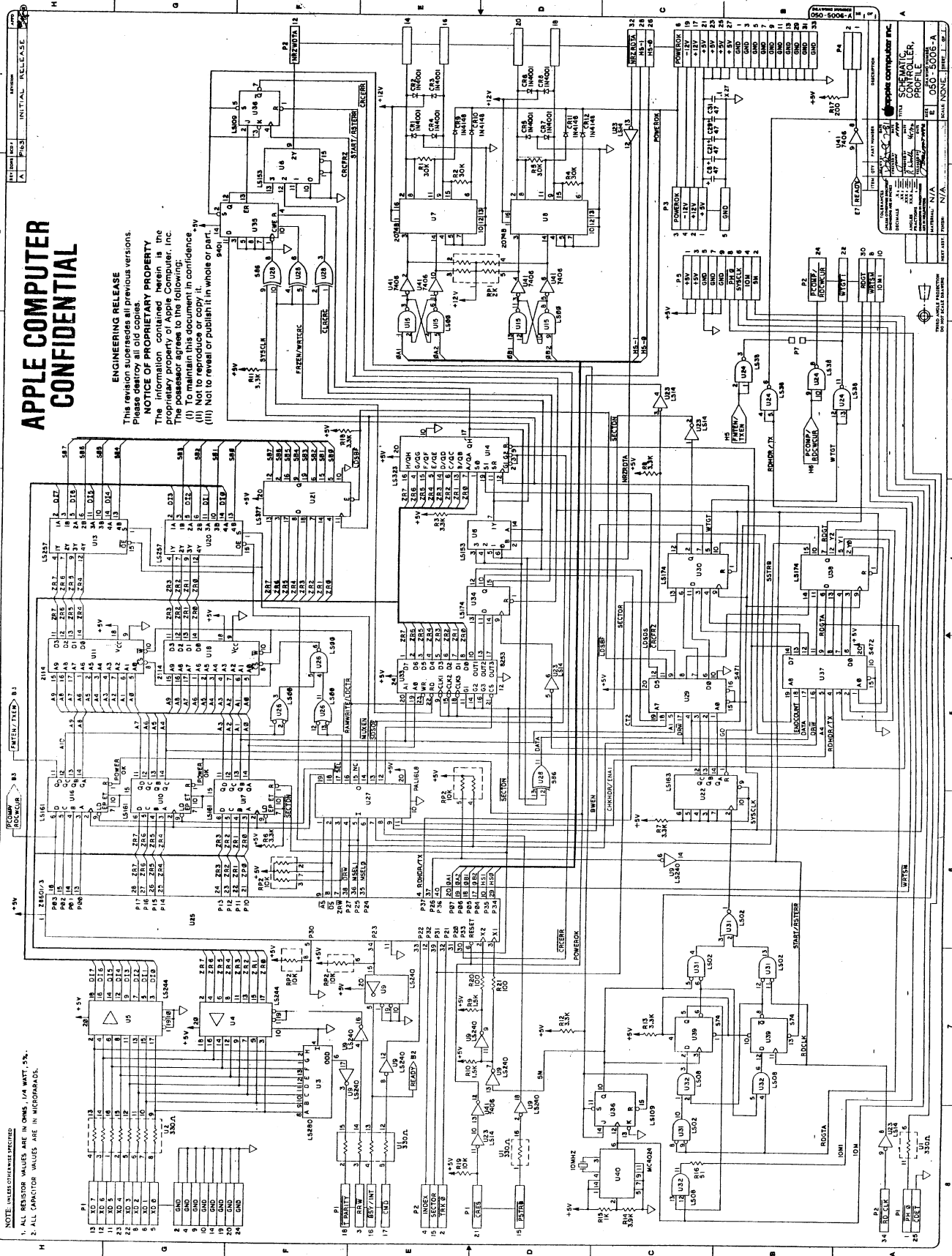
JUMPER-INSERT FOR TESTING OUT OF SYSTEM

ADDITIONAL BYPASS AS REV'D
C1-C3, C21, C38 ARE ADD'L 0.1 μF CAPS
ALL ON +5V



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1. ALL RESISTOR VALUES ARE IN OHMS, 1/4 WATT, 5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.

Apple Computer Inc.
SHEWAN TOMES & CO. LTD.
SCHEMATIC
DRAWN BY: [Name]
CHECKED BY: [Name]
DATE: [Date]
PART NO: 0057-0058-A
REV: 1

