

Table H-10 (continued)
Address register bits Interpretation

Address	Register	Bits	Interpretation
\$C08B+s0	CONTROL		ACIA control register (read/write).
		0–3	Baud rate: \$00 = 16 times external clock; see Table H-1.
		4	When 1, use baud rate generator; when 0, use external clock (not supported).
		5–6	Number of data bits: 8 (bit 5 and 6 = 0) 7 (5 = 1, 6 = 0), 6 (5 = 0, 6 = 1) or 5 (bit 5 and 6 both = 1).
		7	Number of stop bits: 1 if bit 7 = 0; if bit 7 = 1, then 1-1/2 (with 5 data bits, no parity), 1 (8 data plus parity), or 2

Scratchpad RAM locations

The SSC uses the scratchpad RAM locations listed in Table H-11.

Table H-11
Scratchpad RAM locations used by the SSC

Address	Field name	Bit	Interpretation
\$0478+s	DELAYFLG	0–1	Form feed delay selection.
		2–3	Line feed delay selection.
		4–5	Carriage return delay selection.
		6–7	Translate option.
\$04F8+s	PARAMETE	0-7	Accumulator for firmware's command processor.
\$0578+s	STATEFLG	0–2	Command mode when not 0.
		3–5	Slot to chain to (communications mode).
		6	Set to 1 after lowercase input character.
		7	Terminal mode when 1 (communications mode).
		7	Enable CR generation when 1 (printer mode).