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## 65C02 timing

The operation of the Apple IIe is controlled by a set of synchronous timing signals, sometimes called *clock signals*. In electronics, the word *clock* is used to identify signals that control the timing of circuit operations. The Apple IIe doesn't contain the kind of clock you tell time by, although its internal timing is accurate enough that a program running on the Apple IIe can simulate such a clock.

The frequency of the oscillator that generates the master timing signal is 14.31818 MHz. Circuitry in the Apple IIe uses this clock signal, named 14M, to produce all the other timing signals. These timing signals perform two major tasks: controlling the computing functions, and generating the video display. The timing signals directly involved with the operation of the 65C02 (and 6502 on the original version of the Apple IIe) are described in this section. Other timing signals are described in this chapter in the sections "RAM Addressing," "Video Display Modes," and "The Expansion Slots."

The main 65C02 timing signals are listed in Table 7-5, and their relationships are diagrammed in Figure 7-1. The 65C02 clock signals are  $\phi 1$  and  $\phi 0$ , complementary signals at a frequency of 1.02273 MHz. The Apple IIe signal named  $\phi 0$  is equivalent to the signal called  $\phi 2$  in the hardware manual. (It isn't identical: it's a few nanoseconds early.)

The operations of the 65C02 are related to the clock signals in a simple way: address during  $\phi 1$ , data during  $\phi 0$ . The 65C02 puts an address on the address bus during  $\phi 1$ . This address is valid not later than 140 nanoseconds after  $\phi 1$  goes high and remains valid through all of  $\phi 0$ . The 65C02 reads or writes data during  $\phi 0$ . If the 65C02 is writing, the read/write signal is low during  $\phi 0$  and the 65C02 puts data on the data bus. The data is valid not later than 75 nanoseconds after  $\phi 0$  goes high. If the 65C02 is reading, the read/write signal remains high. Data on the data bus must be valid no later than 50 nanoseconds before the end of  $\phi 0$ .