

## ■ OPERATIONAL CODES, EXECUTION TIME, AND MEMORY REQUIREMENTS

		IMME	ABSUTE	ZERO	ACCUM	IM-	(IND,	(IND,						RELAT	(ABS)	ABS	(ZPG)	PROCESSOR																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
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**Notes:**

- |  |   |                |                             |
|--|---|----------------|-----------------------------|
| 1. Add 1 to "n" if page boundary is crossed.   | X Index X                               | + Add          | n No. Cycles                |
| 2. Add 1 to "n" if branch occurs to same page.   | Y Index Y                               | - Subtract     | n No. Bytes                 |
| 3. Add 2 to "n" if branch occurs to different page.  | A Accumulator                           | Λ And          | M <sub>6</sub> Memory bit 6 |
| 3. Add 1 to "n" if decimal mode.   | M Memory per effective address          | V Or           | M <sub>7</sub> Memory bit 7 |
| 4. V bit equals memory bit 6 prior to execution.   | M <sub>s</sub> Memory per stack pointer | ⊕ Exclusive or |                             |
| N bit equals memory bit 7 prior to execution.  |   |                |                             |
| 5. The immediate addressing mode of the BIT instruction leaves bits 6 & 7 (V & N) in the Processor Status Code Register unchanged. |   |                |                             |