

Table 7-9
RAM address multiplexing

Mux'd address	Row address	Column address
RA0	A0	A9
RA1	A1	A6
RA2	A2	A10
RA3	A3	A11
RA4	A4	A12
RA5	A5	A13
RA6	A7	A14
RA7	A8	A15

Now consider how the display is refreshed. As described later in this chapter in the section "The Video Counters," the display circuitry generates a sequence of 8,192 memory addresses in high-resolution mode; in text and low-resolution modes, this sequence is the 1,024 display-page addresses repeated eight times. The display address cycles through this sequence 60 times a second, or once every 17 milliseconds. The way the low-order address lines are assigned to the RAMs, the row address cycles through all 256 possible values once every two milliseconds. (See Figure 7-11.) This more than satisfies the refresh requirements of the dynamic RAMs.

Dynamic-RAM timing

The Apple IIe's microprocessor clock runs at a moderate speed, about 1.023 MHz, but the interleaving of CPU and display cycles means that the RAM is being accessed at a 2 MHz rate, or a cycle time of just under 500 nanoseconds. Data for the CPU is strobed by the falling edge of $\phi 0$, and display data is strobed by the falling edge of $\phi 1$, as shown in Figure 7-11.

The RAM timing looks complicated because the RAM address is multiplexed, as described in the previous section. The MMU takes care of multiplexing the address for the CPU cycle, and the IOU performs the same function for the display cycle. The multiplexed address is sent to the RAM ICs over the lines labeled RA0–RA7. Along with the other timing signals, the PAL device generates two signals that control the RAM addressing: row-address strobe (RAS) and column-address strobe (CAS).