

Table 7-8 (continued)
PAL signal descriptions

Pin	Signal	Description
10	GND	Power and signal common
11	ENTMG	Enable master timing
12	LDPS'	Video shift-register load enable
13	VID7M	Video dot clock, 7 or 14 MHz
14	==1	Phase 1 system clock
15	ø0	Phase 0 system clock
16	Q3	Intermediate timing and strobe signal
17	PCAS'	RAM column-address strobe
18	N.C.	(This pin is not used.)
19	PRAS'	RAM row-address strobe
20	+5V	Power

Memory addressing

The Apple IIe's microprocessor can address 65,536 locations. Apple IIe uses this entire address space, and then some: some areas in memory are used for more than one function. The following sections describe the memory devices used in the Apple IIe and the way they are addressed. Input and output also use portions of the memory address space; refer to the section "Peripheral-Card Memory Spaces" in Chapter 6 for information.

ROM addressing

In the original and the enhanced Apple IIe's, the following programs are permanently stored in two type 2364 8K by seven-bit ROMs (read-only memory):

- ☐ Applesoft editor and interpreter
- ☐ System Monitor
- ☐ 80-column display firmware
- ☐ self-test routines

These two ROMs are enabled by two signals named ROMEN1 and ROMEN2. The ROM enabled by ROMEN1, sometimes called the *Diagnostics ROM*, occupies the memory address space from \$C100 to \$DFFF. The address space from \$C300 to \$C3FF and from \$C800 to \$CFFF contains the 80-column display firmware. Those address spaces are normally assigned to ROM on a peripheral card in slot 3.

+5V	1	28	+5V
A12	2	27	+5V
A7	3	26	+5V
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	ROMENx'
A2	8	21	A10
A1	9	20	CE'
A0	10	19	MD7
MD0	11	18	MD6
MD1	12	17	MD5
MD2	13	16	MD4
GND	14	15	MD3

Figure 7-5
2364 ROM pinouts