

Table H-10 (continued)
Address register bits Interpretation

Address	Register	Bits	Interpretation
\$C082+s0	DIPSW2 (SW2-x)	0	Clear To Send (CTS) is true when 0.
		1-3	Same as above for SW2-5 through SW2-3.
		5,7	Same as above for SW2-2 and SW-2-1.
\$C088+s0	TDREG	0-7	ACIA transmit register (write).
	RDREG	0-7	ACIA receive register (read).
\$C089+s0	STATUS		ACIA status/reset register.
		0	Parity error detected when 1.
		1	Framing error detected when 1.
		2	Overrun detected when 1.
		3	ACIA receive register full when 1.
		4	ACIA transmit register empty when 1.
		5	Data Carrier Detect (DCD) true when 0.
		6	Data Set Ready (DSR) true when 0.
		7	Interrupt (IRQ) has occurred when 1.
\$C08A+s0	COMMAND		ACIA command register (read/write).
		0	Data Terminal Ready (DTR): enable (1) or disable (0) receiver and all interrupts.
		1	When 1, allow STATUS bit 3 to cause interrupt.
		2-3	Control transmit interrupt, Request To Send (RTS) level, and transmitter.
		4	When 0, normal mode for receiver; when 1, echo mode (but bits 2 and 3 must be 0).
		5-7	Control parity.