



**Figure 7-11**  
RAM timing signals

**Table 7-10**  
RAM timing signal descriptions

Signal	Description
$\phi_0$	Clock phase 0 (CPU phase)
$\phi_1$	Clock phase 1 (display phase)
RAS	Row-address strobe
CAS	Column-address strobe
Q3	Alternate RAM/column-address strobe
RA0-RA7	Multiplexed address bus
MD0-MD7	Internal data bus