apple II product specifications

hobby/prototyping board

GENERAL DESCRIPTION

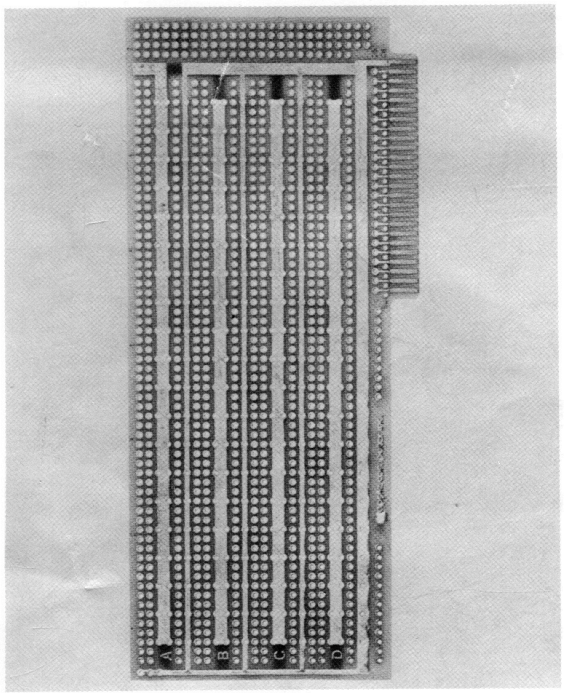
The APPLE II Hobby/Peripheral Board is a 2-3/4" x 7" two sided printed circuit board with a hole pattern on 100 mil centers. The board will accept all conventional integrated circuit packages as well as transistors, resistors, capacitors and other passive components. It is intended for use as a means of breadboarding experimental circuitry or a unique interface for a computer peripheral or hobby accessory.

FEATURES

- Row and Column Alpha Numeric identification for easy layout reference
- Heavy duty power and ground bus
- Hole pattern on 100 mil grid for any size IC
- Gold Plated contacts
- Computer grade board
- Wire wrap or point to point interconnect

ORDERING INFORMATION

Order Product Code A2B0001X



Board Photograph

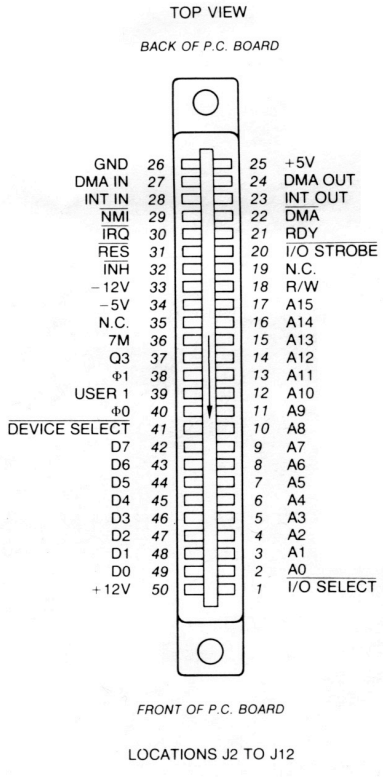


Figure 1. Peripheral Connector Pinout

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030-0007-00

TABLE I

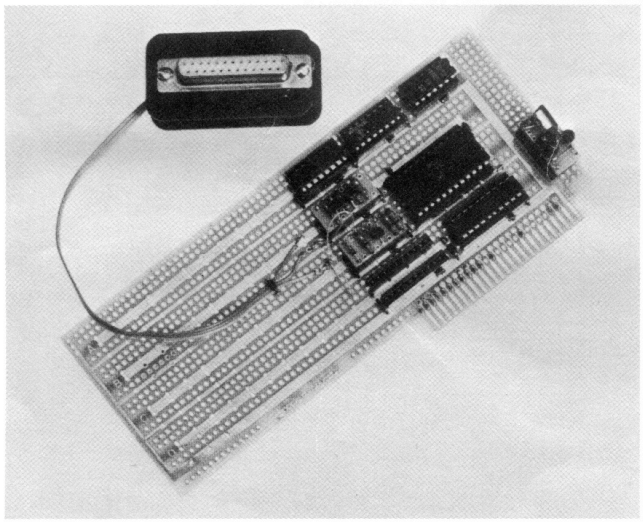
SIGNAL DESCRIPTION FOR PERIPHERAL I/O CONNECTORS

Pin #	Pin Name	Description
1	I/O SELECT	256 addresses are set aside for each peripheral connector (see address map). A read or write at such an address will send Pin 1 on the selected connector low during ϕ_0 (500ns). This line is not available on peripheral connector 0. Refer to Table II for address allocation.
2-17	A_0-A_{15}	16-bit system address bus. Addresses are set up by the 6502 within 300ns after the beginning of ϕ_1.
18	R/$\overline{W}$	READ/$\overline{WRITE}$ line from 6502. When high indicates that a read cycle is in progress, and when low that a write cycle is in progress.
19	NC	No connection.
20	$\overline{I/O\ STROBE}$	Pin 20 on all peripheral connectors will go low during ϕ_0 of a read or write to any address $C800-$CFFF. Refer to Table II for address allocation.
21	RDY	"Ready" line to the 6502. This line should change only during ϕ_1, and when low will halt the microprocessor at the next READ cycle. This line has a 3KΩ pullup to +5V.
22	$\overline{DMA}$	Direct Memory Access control output. This line has a 3KΩ pullup to +5V.
23	INT OUT	Interrupt daisy chain output to lower priority peripheral devices. Note: Pins 28 and 23 must be connected together if not used on the card.
24	DMA OUT	Direct Memory Access daisy chain output to lower priority peripheral devices. Note: Pins 27 and 24 must be connected together if not used on the card.
25	+5V	Positive 5-volt supply*, 500 mA total for all peripheral boards together.
26	GND	System circuit ground. 0 volt line from power supply.
27	DMA IN	Direct Memory Access daisy chain input from higher priority peripheral devices. Usually connected to Pin 22.
28	INT IN	Interrupt daisy chain input from higher priority peripheral devices. Usually connected to Pin 23.
29	NMI	Non Maskable Interrupt request line to the 6502. This line has a 3KΩ pullup to +5V. It is active low.
30	$\overline{IRQ}$	Interrupt request line to the 6502. This line has a 3KΩ pullup to +5V. It is active low.
31	$\overline{RES}$	Reset line from "RESET" key on keyboard. Active low.
32	$\overline{INH}$	Inhibit Line. When a device pulls this line low, all ROM's on board are disabled (Hex addressed $D000 through $FFFF). This line has a 3KΩ pullup to +5V.
33	-12V	Negative 12 volt supply*, 200mA total for all peripheral boards together.
34	-5V	Negative 5 volt supply*, 200 mA total for all peripheral boards together.
35	NC	No connection.
36	7M	Seven MHz high frequency clock.
37	Q_3	A 2MHz (nonsymmetrical) general purpose timing signal.
38	ϕ_1	Phase 1 clock, complement of ϕ_0 clock.
39	USER 1	The function of this line will be described in a later document.
40	ϕ_0	Microprocessor phase ϕ_0 clock.

Table I (Continued)

Pin #	Pin Name	Description
41	$\overline{\text{DEVICE SELECT}}$	Sixteen addresses are set aside for each peripheral connector. A read or write to such an address will cause Pin 41 on the selected connector to go low during ϕ_0 (500ns). Refer to Table II for address allocation.
42-49	D_0-D_7	8-bit system data bus. During a write cycle, data is set up by the 6502 less than 300ns after the beginning of ϕ_2. During a read cycle the 6502 expects data to be ready no less than 100ns before the end of ϕ_0.
50	+12V	Positive 12 volt supply*, 250mA total for all peripheral boards together.

*Note: Total power drawn by any one peripheral board is not to exceed 1.5 watts.



Typical Hobby Board Configuration

DESIGN TECHNIQUES FOR APPLE II HOBBY BOARDS

GENERAL LAYOUT

Figure 1 is an illustration of an APPLE II peripheral board in an I/O connector. Note that the short end of the board is to the back edge of the system and components are mounted on the side containing the Apple Computer logo. The APPLE II hobby boards are designed to have both +5V and GND available on both sides of the board. If other voltages are used they must be individually wired. The boards are designed for use with either wire-wrap or conventional wiring techniques. IC sockets are generally recommended in hobby applications. TTL should be low power Schottky where possible.

DECOUPLING

All voltages used on the hobby board should be decoupled with a 0.1μf capacitor to ground near the I/O connector board power pin. Additional 0.1μf capacitors should be used for approximately every four low power Schottky, CMOS, or MOS devices. DO NOT USE HIGH VALUE ELECTROLYTIC DECOUPLING CAPACITORS. They can cause improper operation of the APPLE II power supply.

If PROM or buffer power down is used, the power down circuit should be individually decoupled. Do not decouple the switched power pin.

I/O LOADING AND DRIVE RULES

Table II gives the drive and loading requirements for the peripheral I/O connector. The address bus, the data bus, and the R/W lines should be driven by tri-state buffers. The 74LS365 is typically a good choice. Remember that there is considerable capacitance distributed over the board, and one should look forward to tolerating the extra load of seven other peripheral cards. Attempting to use PIA's and ACIA's directly on the bus will generally lead to timing and level errors. Type 2316 ROM's are an exception because the timing allows a very large margin. The drive required and the maximum loading allowed are stated in terms of low power Schottky logic (LSTTL).

TABLE II
LOADING AND DRIVING RULES

Pin Number	Name	Required Drive	Maximum LSTTL Load
1	$\overline{\text{I/O SELECT}}$	N/A	10
2-17	A_0-A_{15}	Tri-State Buffer	5
18	R/$\overline{W}$	Tri-State Buffer	10
19	N/C	N/A	N/A
20	$\overline{\text{I/O STROBE}}$	N/A	2
21	RDY	Open Collector	N/A
22	$\overline{\text{DMA}}$	Open Collector	N/A
23	INT OUT	4 LSTTL	N/A
24	DMA OUT	4 LSTTL	N/A
25	+5V	N/A	N/A
26	GND	N/A	N/A
27	DMA IN	N/A	4
28	INT IN	N/A	4
29	NMI	Open Collector	N/A
30	IRQ	Open Collector	N/A
31	$\overline{\text{RES}}$	N/A	2
32	$\overline{\text{INH}}$	Open Collector	N/A
33	-12V	N/A	N/A
34	-5V	N/A	N/A
35	N/C	N/A	N/A
36	7M	N/A	2
37	Q3	N/A	2
38	ϕ_1	N/A	2
39	USER 1	N/A	N/A
40	ϕ_0	N/A	2
41	$\overline{\text{DEVICE SELECT}}$	N/A	10
42-49	D_0-D_7	Tri-State Buffer	1
50	+12V	N/A	N/A

TIMING SIGNALS

A number of system timing signals are available on the APPLE II Bus. Figure 2 shows the details of the relative timing of the available signals. ϕ_0 on the APPLE II Bus has significant on-board fan-out and should not be used on APPLE II peripherals. Inverting ϕ_1 will provide a safe ϕ_0 signal.

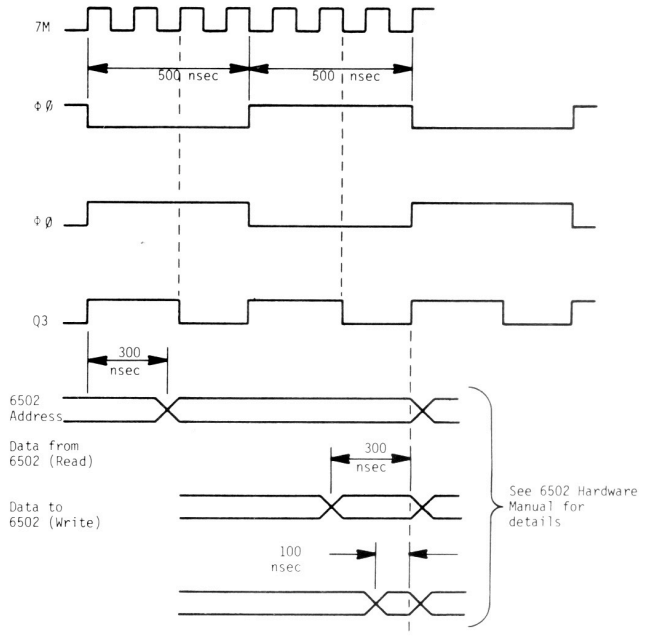


Figure 2. 6502 Timing Diagram

TABLE III
PERIPHERAL ADDRESS ALLOCATION

Hex Address	Assigned Function	Slot Number	Comments
C080-C08F	$\overline{\text{DEVICE SELECT}}$	0	Pin 41 on the selected Peripheral Connector goes low during ϕ_0.
C090-C09F	$\overline{\text{DEVICE SELECT}}$	1	
C0A0-C0AF	$\overline{\text{DEVICE SELECT}}$	2	
C0B0-C0BF	$\overline{\text{DEVICE SELECT}}$	3	
C0C0-C0CF	$\overline{\text{DEVICE SELECT}}$	4	
C0D0-C0DF	$\overline{\text{DEVICE SELECT}}$	5	
C0E0-C0EF	$\overline{\text{DEVICE SELECT}}$	6	
C0F0-C0FF	$\overline{\text{DEVICE SELECT}}$	7	
C100-C1FF	$\overline{\text{I/O SELECT}}$	1	Pin 1 on the selected Peripheral Connector goes low during ϕ_0.
C200-C2FF	$\overline{\text{I/O SELECT}}$	2	NOTE: Peripheral Connector 0 does not get this signal.
C300-C3FF	$\overline{\text{I/O SELECT}}$	3	
C400-C4FF	$\overline{\text{I/O SELECT}}$	4	
C500-C5FF	$\overline{\text{I/O SELECT}}$	5	
C600-C6FF	$\overline{\text{I/O SELECT}}$	6	
C700-C7FF	$\overline{\text{I/O SELECT}}$	7	
C800-CFFF	$\overline{\text{I/O STROBE}}$	ALL	I/O Common Address Space. Pin 20 or all peripheral connectors go low during ϕ_0.

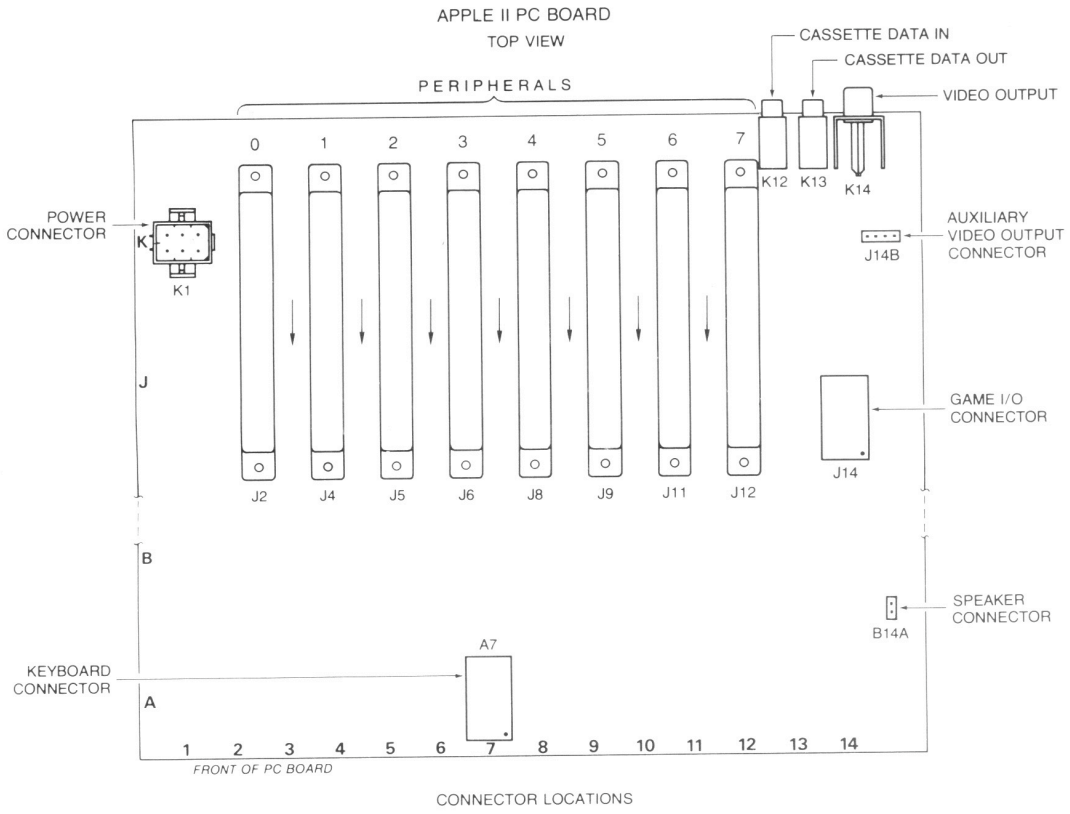


Figure 3. Connector Location Detail

I/O PROGRAMMING SUGGESTIONS

It is usually necessary for the program on an I/O board in $CNXX space use its I/O slot number for indexing into the $C080 + $N0 DEVICE SELECT space and to use the slot dependent RAM locations. The program can determine its own location by using a dummy RTS and getting the return location from the stack. The following is an example of the code:

```
CN08  08        PHP          Save Status
CN09  78        SEI          Disable Interrupt to
                               preserve stack
CN0A  20 58 FF  JSR IORTS    Dummy RTS at FF58
CN0E  BD 00 01  TSX          Load stack pointer
CN11  28        LDA PAGE1,X  Load slot# in accumulator
                PLP          Restore Status
```

The slot number $CN will now be in the accumulator and may be shifted to form $N0 or masked to form $0N. With $N0 in the X register, the DEVICE SELECT addresses may be referenced by:

LDA $C080,X

NOTE: The 6502 will cause a read cycle twice at location $C080 + $N0. The first of these is a false read. Simiarly a store cycle at location $X080 + $N0 will cause a false read cycle followed by the write cycle. These false read cycles can disturb the status register of peripheral devices such as PIA's or ACIA's. Study the 6502 Programming Manual for details on indexed memory operations.

Similarly, with $0N in the Y register, a slot dependent RAM address may be referenced by:

LDA $0478,Y

For this example, if we're dealing with a peripheral in slot 2, the address referenced is $47A. In the same manner, we may access $4FA, $57A, etc. The standard system character input and output subroutines are vectored through switches in RAM. CSW (locations $36 low and $37 high) contains the two-byte address of the current character output subroutine, normally $FDF0 for the APPLE II video display. KSW (locations $38 low and $39 high) contains the two-byte address of the

current character input subroutine, normally $FD1B. Either of these may be changed by the user for dual I/O applications. For example, setting location $36 to $80 and location $37 to $03 will set the current character output entry point as $0380.

Standard character input and output subroutine entry points have been assigned to peripheral slots #1-7:

Slot	Entry
1	$C100
2	$C200
3	$C300
4	$C400
5	$C500
6	$C600
7	$C700

The standard character I/O subroutine entry points may be conveniently placed in CSW (output) and KSW (input) with the BASIC commands PR#N and IN#N respectively, where N is the appropriate slot number. The commands are NP^C (P^C is "control P") and NK^C from monitor. For example, the BASIC command PR #3 sets CSWL (locations $36 and $37) to $C300.

The character output subroutine is passed one character at a time in the A register. On the APPLE II, the parity bit (b7) shall normally be set. This subroutine must return with the A-, X-, and Y- registers, undisturbed, and the decimal mode flag clear for existing software to function.

The character input subroutine expects one character to be passed in the A register. The parity bit should be set to work properly with existing hardware.

Apple Computer has adopted certain conventions pertaining to the use of peripheral select and strobe lines and memory addressing schemes. It is advised that these conventions be reviewed particularly when it is expected that more than one peripheral card will be installed.

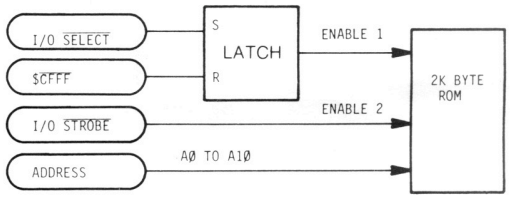
The following discussion applies to peripheral slots number 1 through 7. Slot number 0 is excepted. (See Figure 3).

Pin 1 of the peripheral connector is the I/O SELECT line. This line is active low. It is normally high, and goes low whenever the address bus carries $CNXX, when N equals the peripheral slot number. For example: looking at the peripheral connector number 4, Pin 1 goes low when the address bus reads $C400, or $C401, or $C402 or any hex number from $C400 up through $C4FF. The transition from high to low takes place as ϕ_1 clock line goes low (plus the prop delays through the LS138 decoding logic at F-12 and H-12). One intended use for this line is the chip select for the peripheral card's PROM.

Pin 41 of the peripheral connector is the $\overline{\text{DEVICE SELECT}}$ line. This line is active low, and is derived from the same decoding chain as the I/O SELECT line in an additional LS138 (located at H-2). $\overline{\text{DEVICE SELECT}}$ is normally high, and goes low whenever the address bus carries $C0MX, where $M is 8 plus the peripheral slot number (i.e.: $M = $8 + $N). For example, Pin 41 goes low at peripheral connector number 4 for addresses $C0C0 through $C0CF and for connector number 5, Pin 41 goes low for addresses $C0D0 through $C0DF, and so on. The intended use for this line is the chip select for the peripheral card's ACIA, PIA and other "controller" IC's.

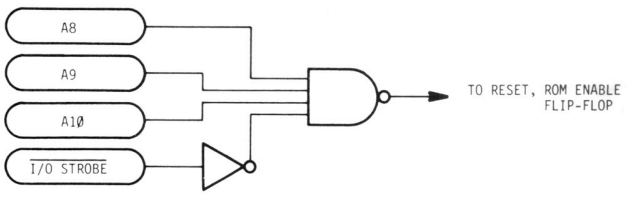
Pin 20 of the peripheral connector is the $\overline{\text{I/O STROBE}}$ line, and is common to all the peripheral connectors. This line is active low and is derived from the LS138 (located at F-12). All peripheral Pin 20's go low when the address bus carries any address within the range $C800 to $CFFF, inclusive. The intended use of this line is for ROM and PROM expansion, and the address $CFFF is allocated to disable the expansion scheme. The following diagram represents such a scheme.

Figure 4.



To simplify decoding the ROM enable RESET, the following scheme can be implemented. By giving up access to 256 bytes out of the 2K bytes of the ROM and using the $\overline{\text{I/O STROBE}}$ line, the hardware requirement is reduced to the following:

Figure 5.



PERIPHERAL SCRATCHPAD MEMORY

Certain areas of RAM are set aside for peripheral RAM storage. The specific addresses are shown in the table below (all are hex).

Location $7F8 is a special one. This location should be loaded with $CN, where N is the slot number of the active peripheral, whenever an interrupt may occur and the ROM/PROM expansion scheme is in use. This is necessary so that the return from interrupt software used allows the proper peripheral card to resume operation.

Common Scratchpad Address	Peripheral Slot Number						
	1	2	3	4	5	6	7
478	479	47A	47B	47C	47D	47E	47F
4F8	4F9	4FA	4FB	4FC	4FD	4FE	4FF
578	579	57A	57B	57C	57D	57E	57F
5F8	5F9	5FA	5FB	5FC	5FD	5FE	5FF
678	679	67A	67B	67C	67D	67E	67F
6F8	6F9	6FA	6FB	6FC	6FD	6FE	6FF
788	779	77A	77B	77C	77D	77E	77F
7F8*	7F9	7FA	7FB	7FC	7FD	7FE	7FF