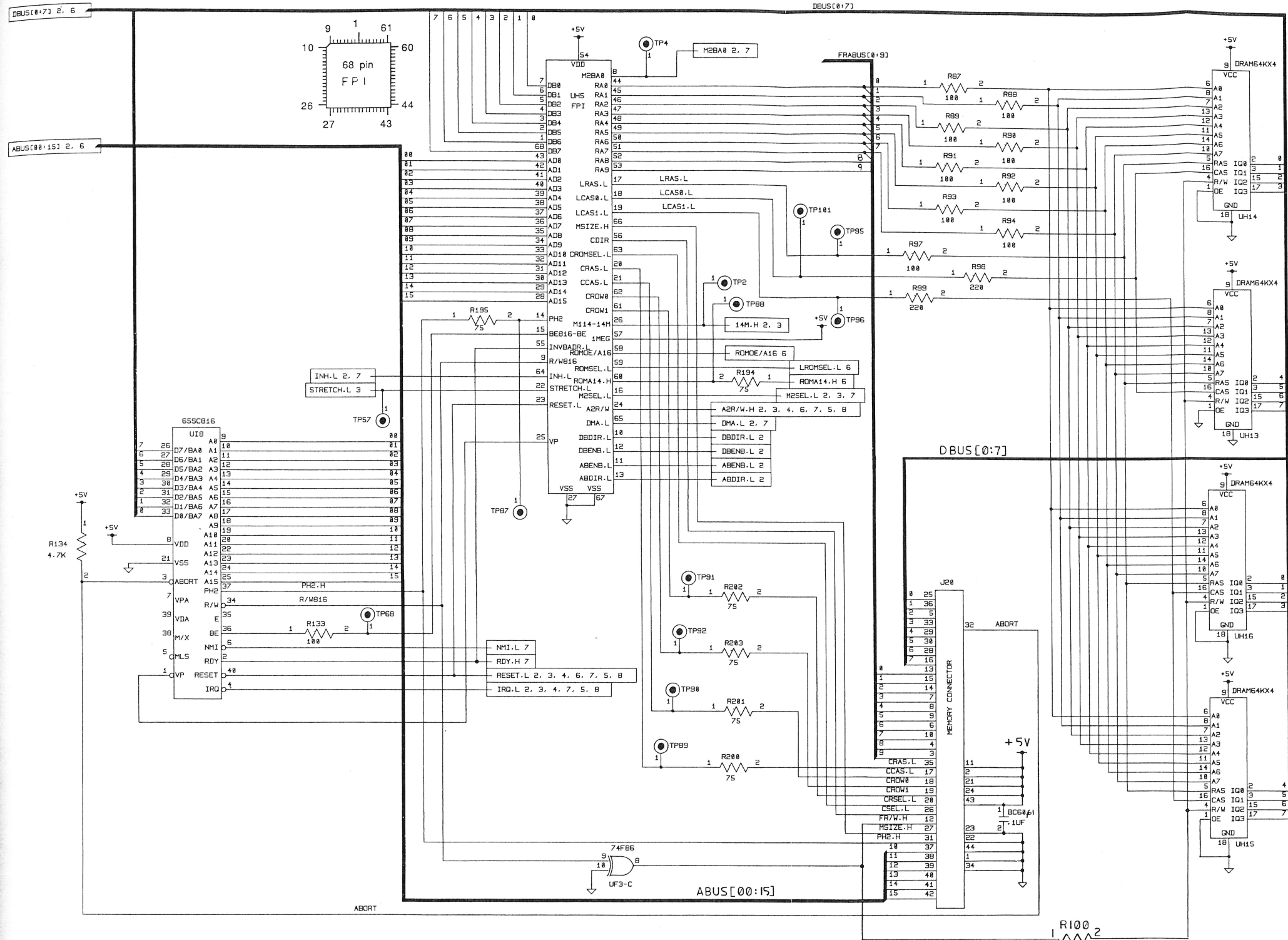
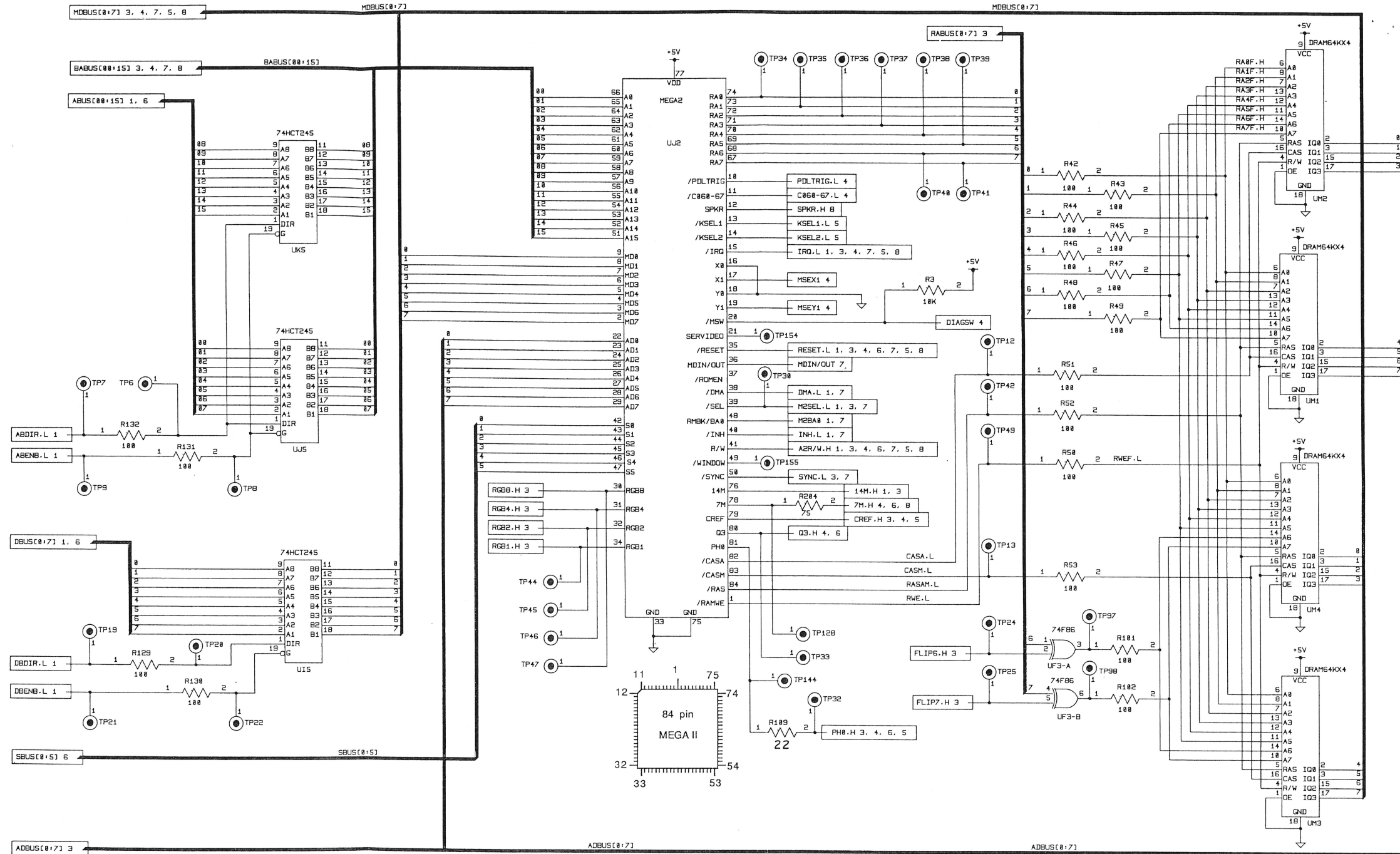


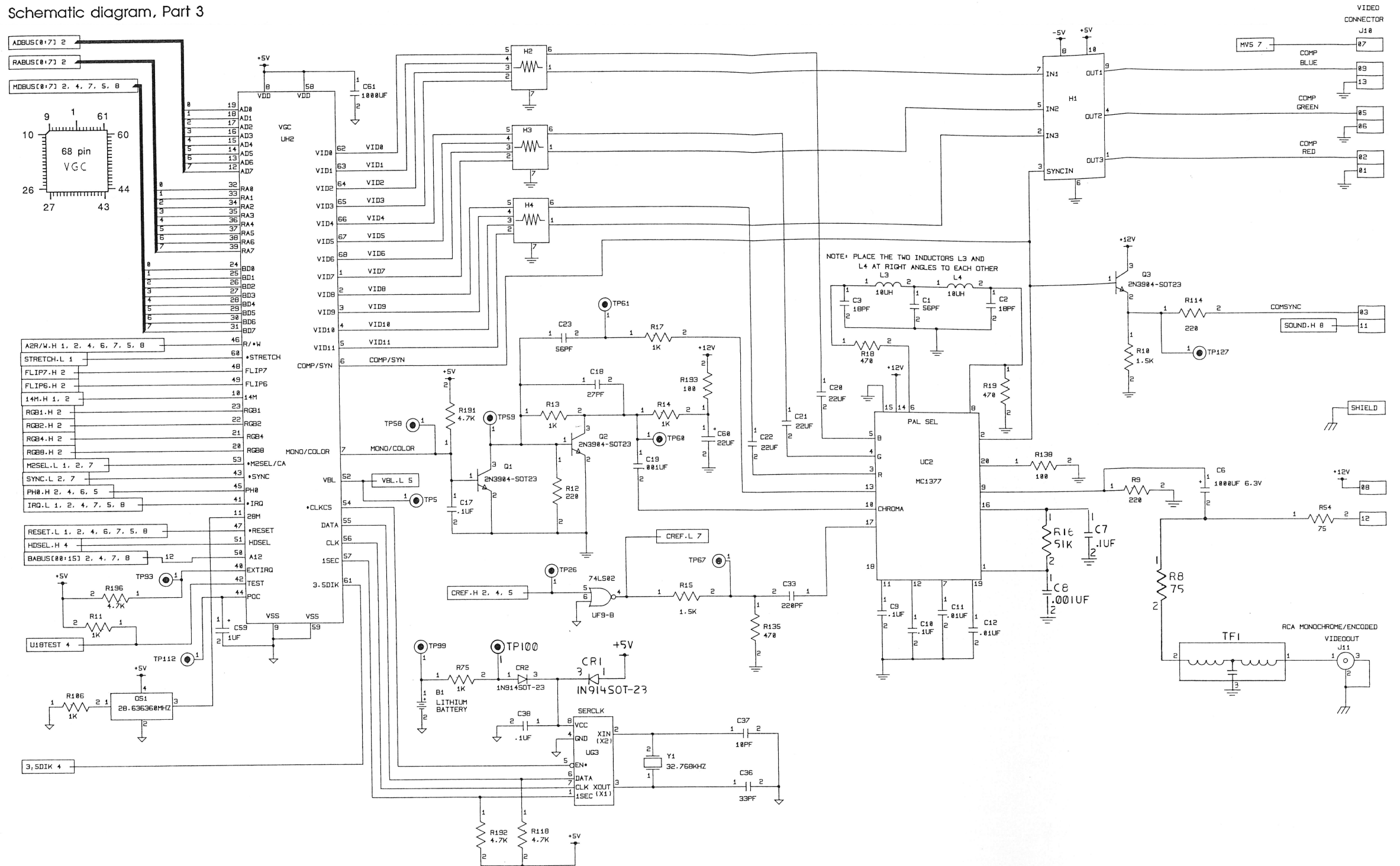
Schematic diagram, Part 1



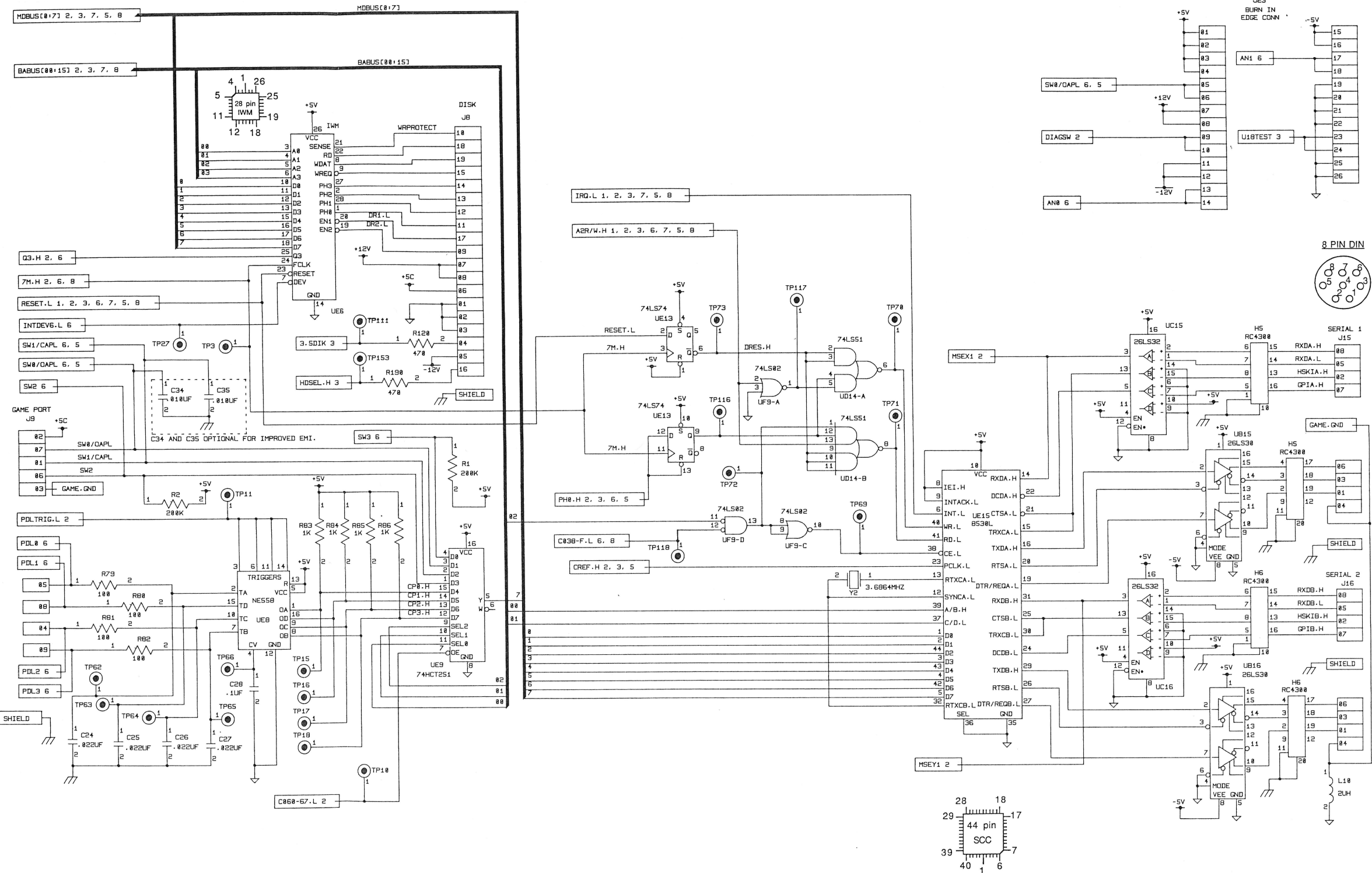
Schematic diagram, Part 2



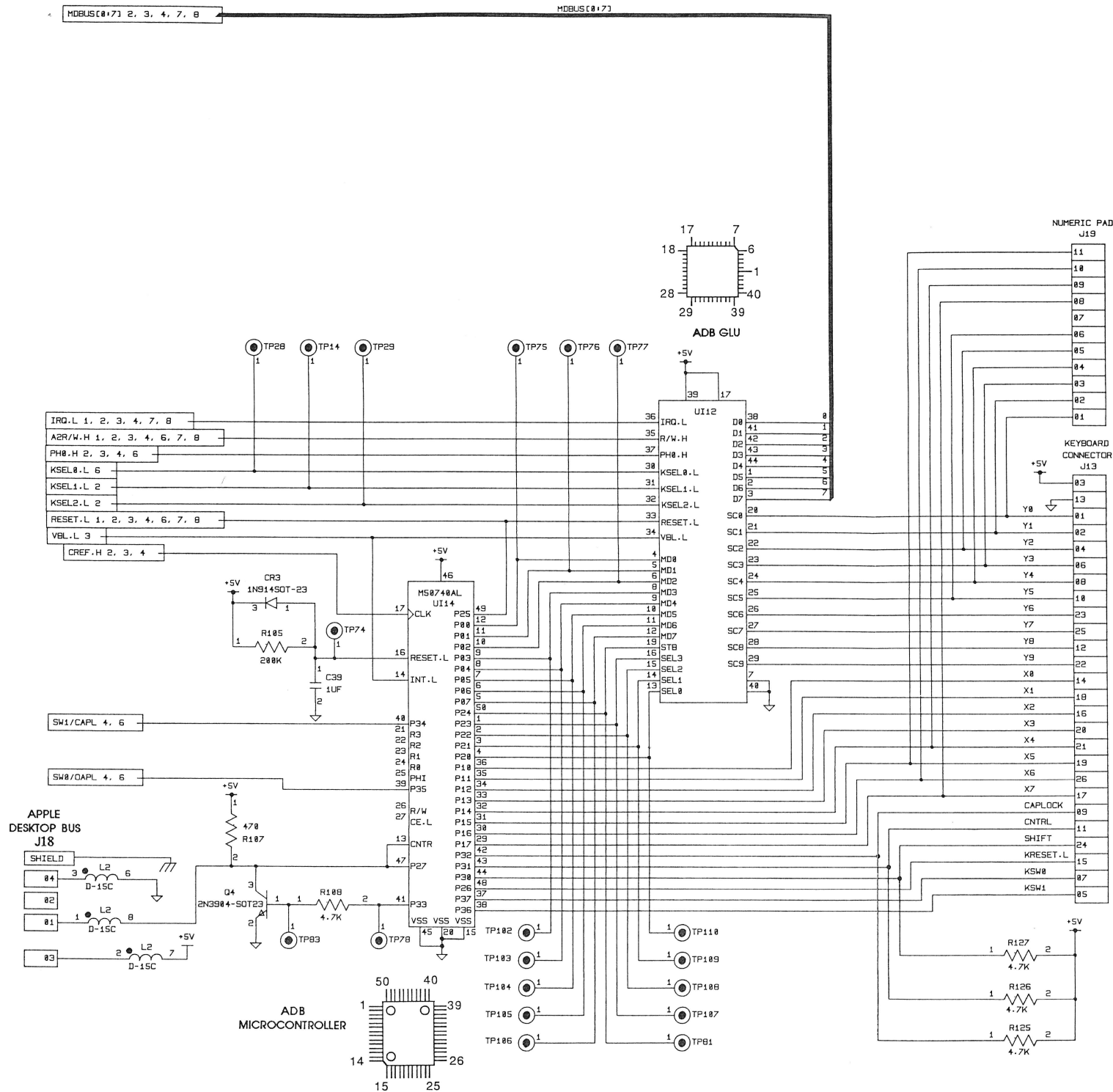
Schematic diagram, Part 3



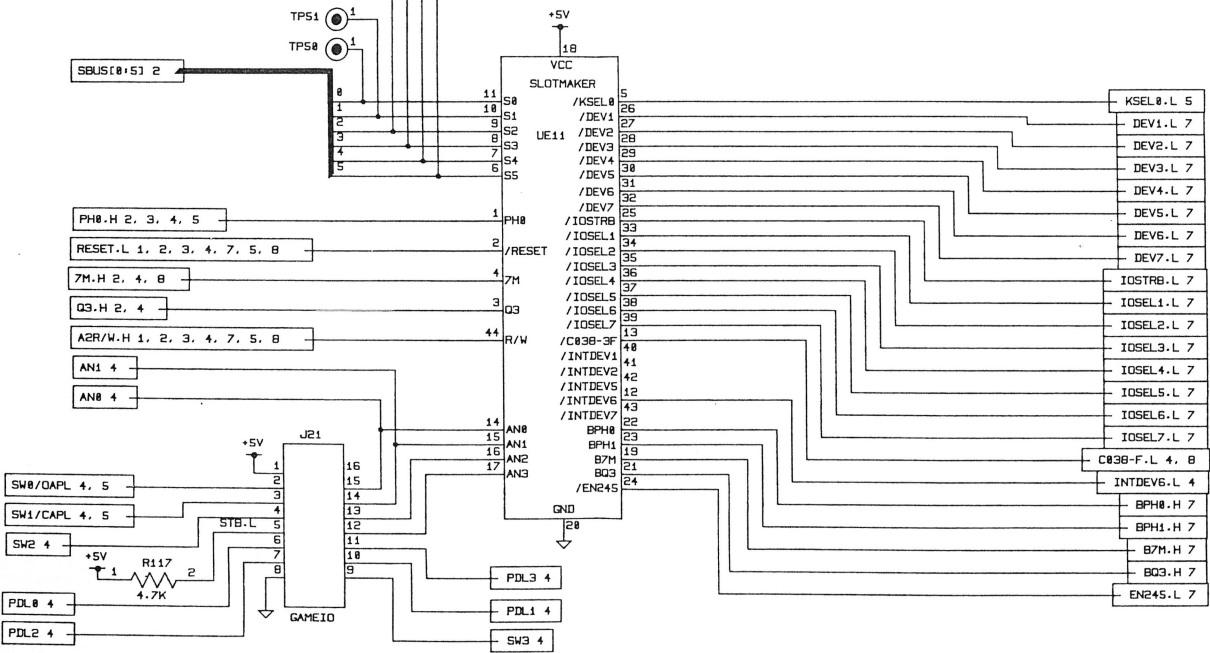
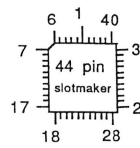
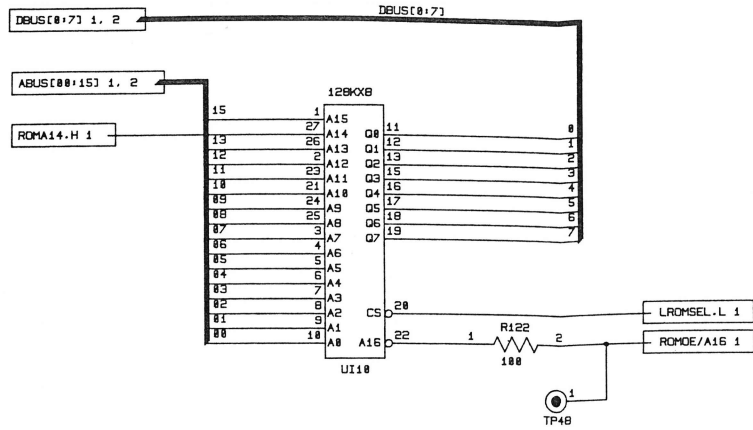
Schematic diagram, Part 4



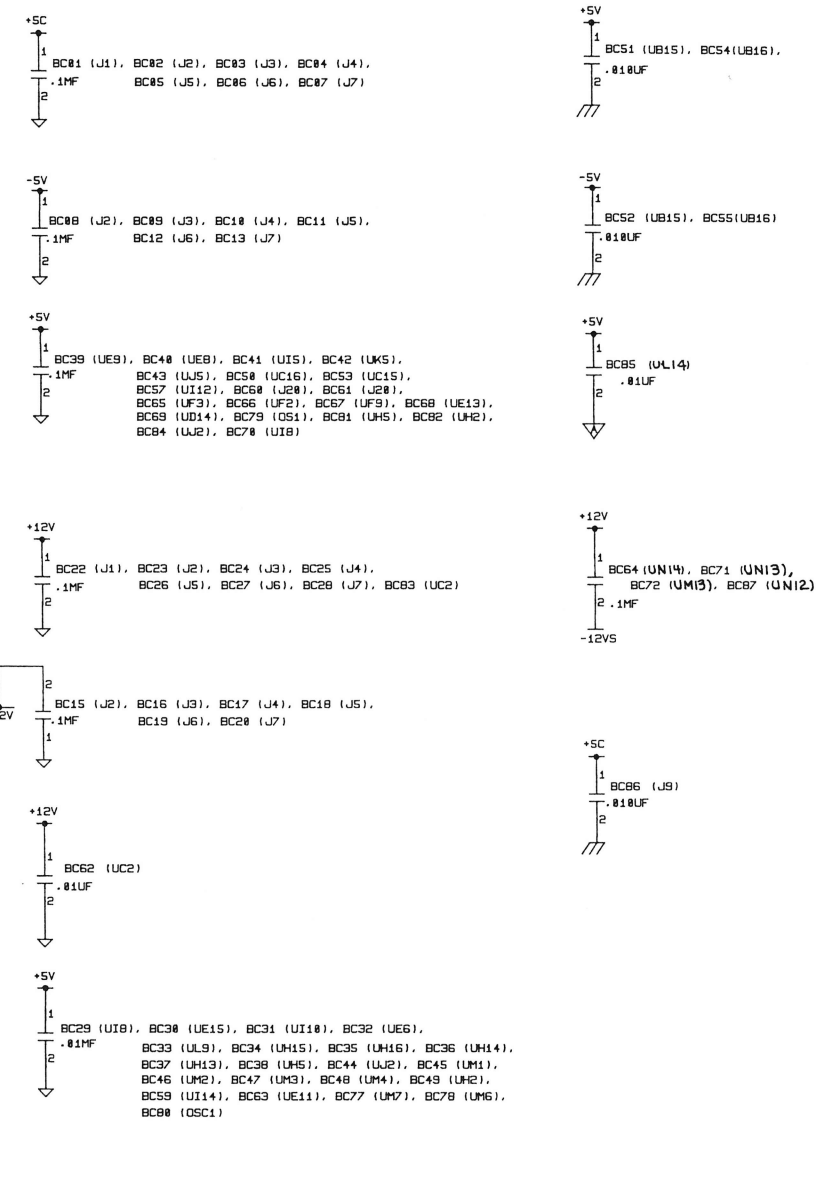
Schematic diagram, Part 5



Schematic diagram, Part 6



BYPASS CAPACITORS



A2R

IOS1

RDY

DMA

NMI

IRQ

RES

INH

M2B

B7M

BQ3

BPH

M2S

BPH

DE

MD

MD

EN

FA

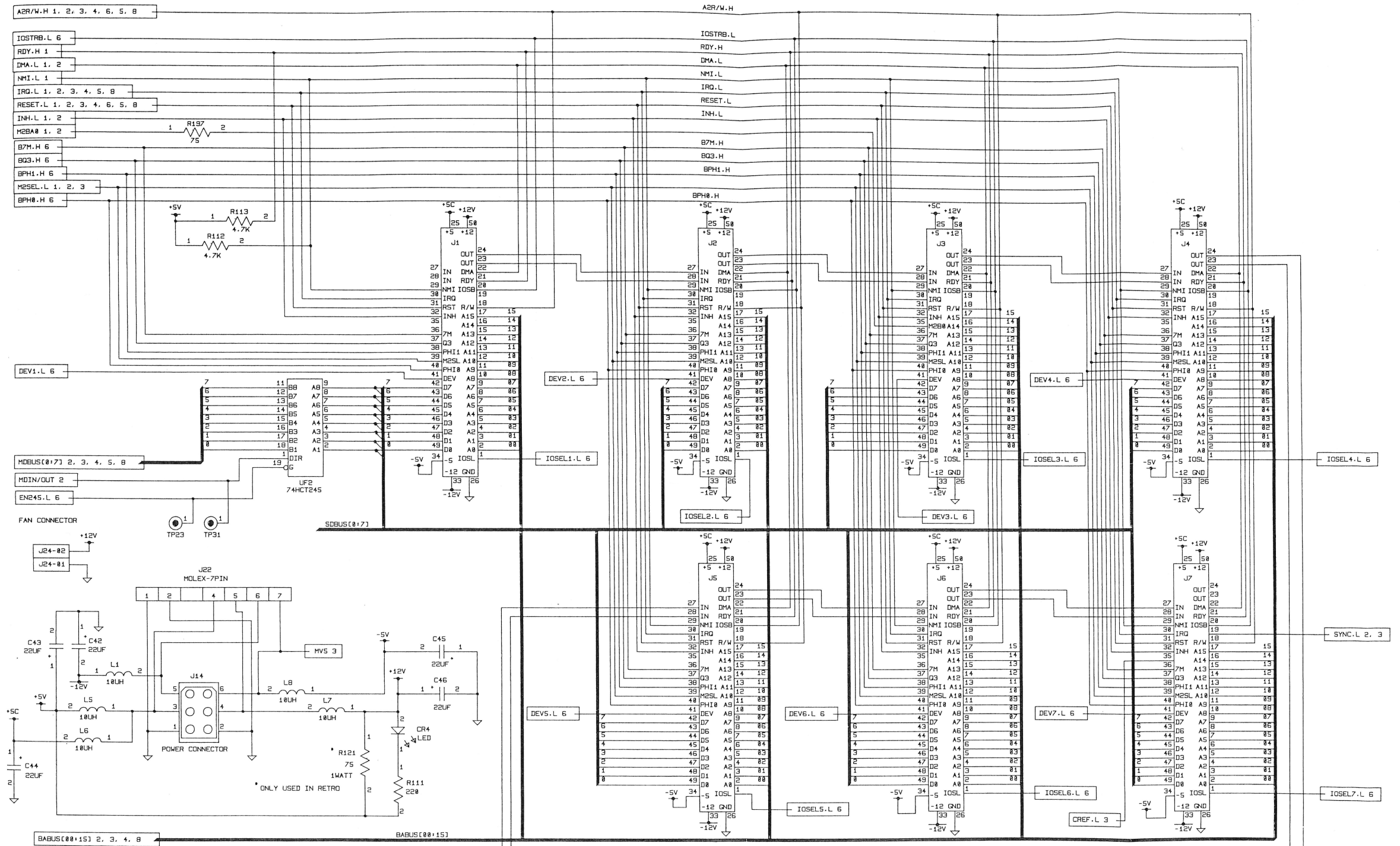
+5C

1

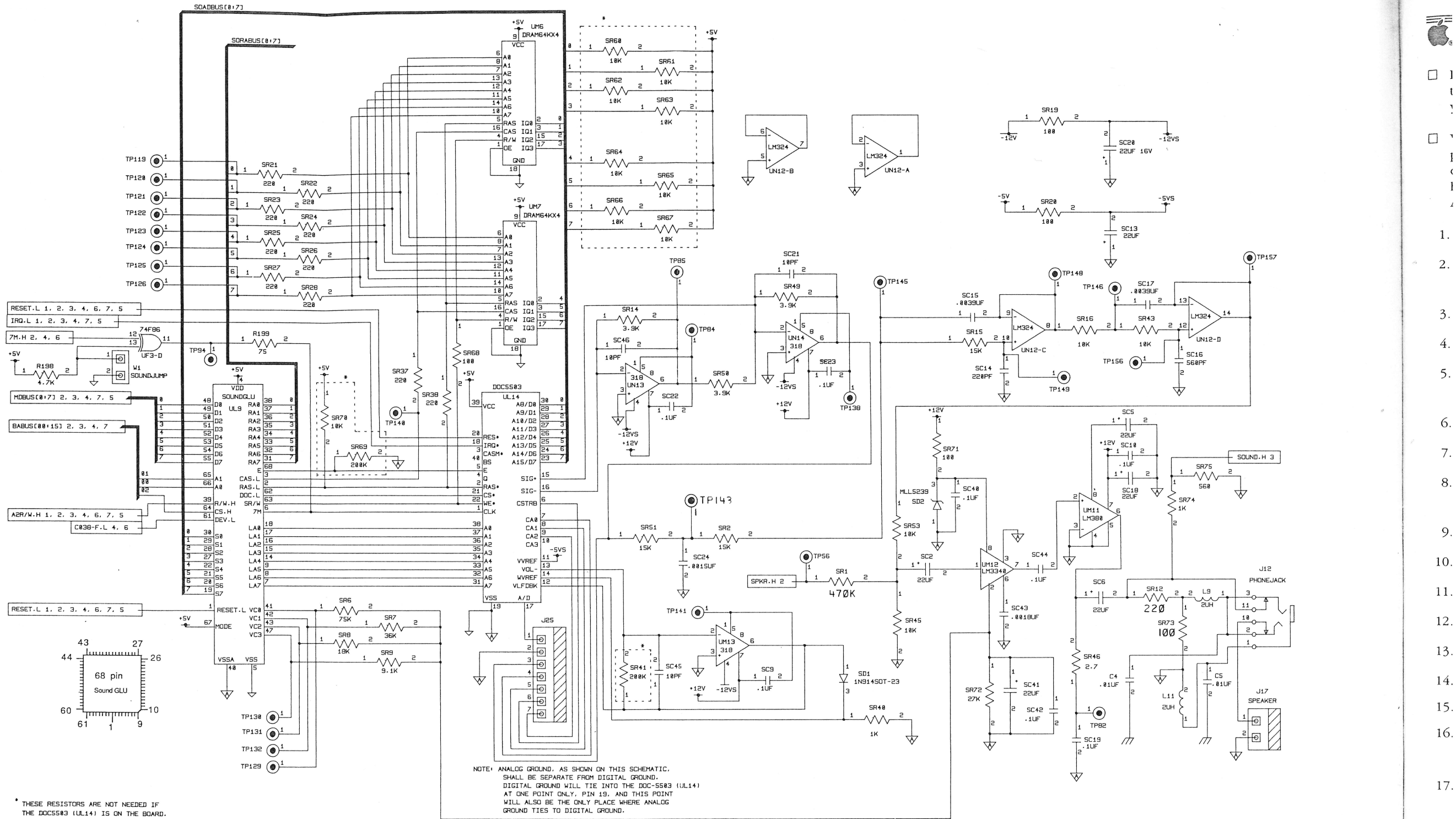
2

2

Schematic diagram, Part 7



Schematic diagram, Part 8



NOTE: ANALOG GROUND, AS SHOWN ON THIS SCHEMATIC, SHALL BE SEPARATE FROM DIGITAL GROUND. DIGITAL GROUND WILL TIE INTO THE DOC-5503 (UL14) AT ONE POINT ONLY, PIN 19, AND THIS POINT WILL ALSO BE THE ONLY PLACE WHERE ANALOG GROUND TIES TO DIGITAL GROUND.

* THESE RESISTORS ARE NOT NEEDED IF THE DOC5503 (UL14) IS ON THE BOARD.

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