

To celebrate the Apple IIgs 13th Birthday this month, GS WorldView is presenting this personal GIF scans set of the IIgs motherboard schematic diagrams in our September, 1999 Issue.

### Graphic File Information

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File Format: GIF 87a  
Color Palette: B/W (1 Bit)  
Resolution: 72x72dpi  
Compression: 1:5 or 1:7

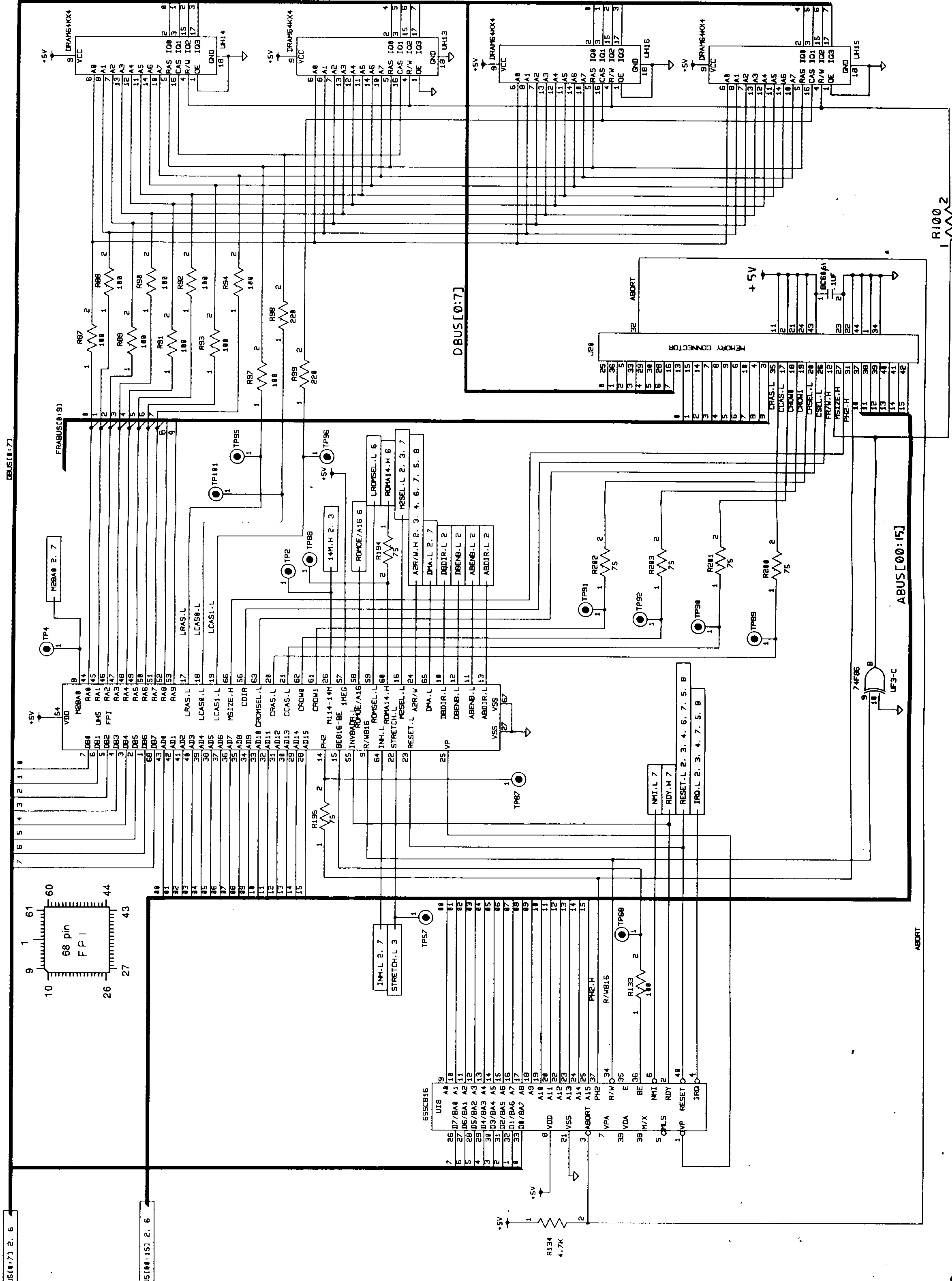
The IIgs motherboard schematic diagrams set is presented in eight parts. Some of the eight parts were scanned as a single graphic GIF file and some were scanned as two graphic GIF files to allow viewing of the entire IIgs motherboard schematic diagram for each part.

Reference examples: PART1.GIF  
PART3.A.GIF and PART3.B.GIF

Each GIF file is Copyright ©1999 by MacProber and GS WorldView. They may be used by anybody for their needs without restrictions. You may notice some of the GIF files are at a bit of an angle. Sorry, this was the way the scan worked to compensate for the large size of each part when done in two GIF scans.

These GIF files should be able to present the entire IIgs motherboard schematic diagrams with enough clarity and detail to allow you to use them with any of the GIF view programs for the Apple IIgs and other Apple II models. They can of course, be viewed with any other computer platform also.

Schematic diagram, Part 1



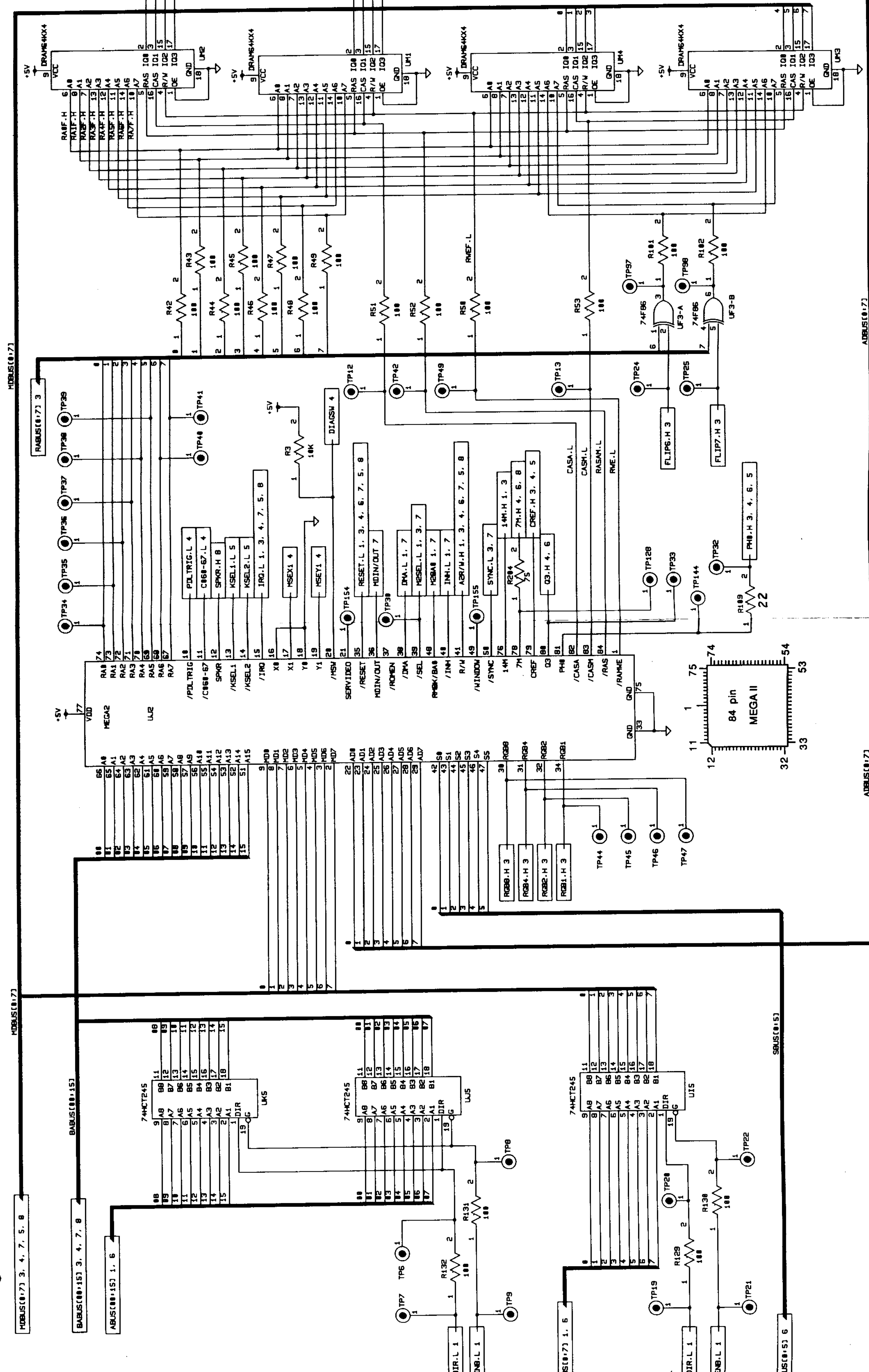
DBUS[0:7] 2. 6

ABUS[00:15] 2. 6

DBUS[0:7]

ABUS[00:15]

ABORT



MDBUS[0:7]

MDBUS[0:7]

MDBUS[0:7]

ADBUS[0:7]

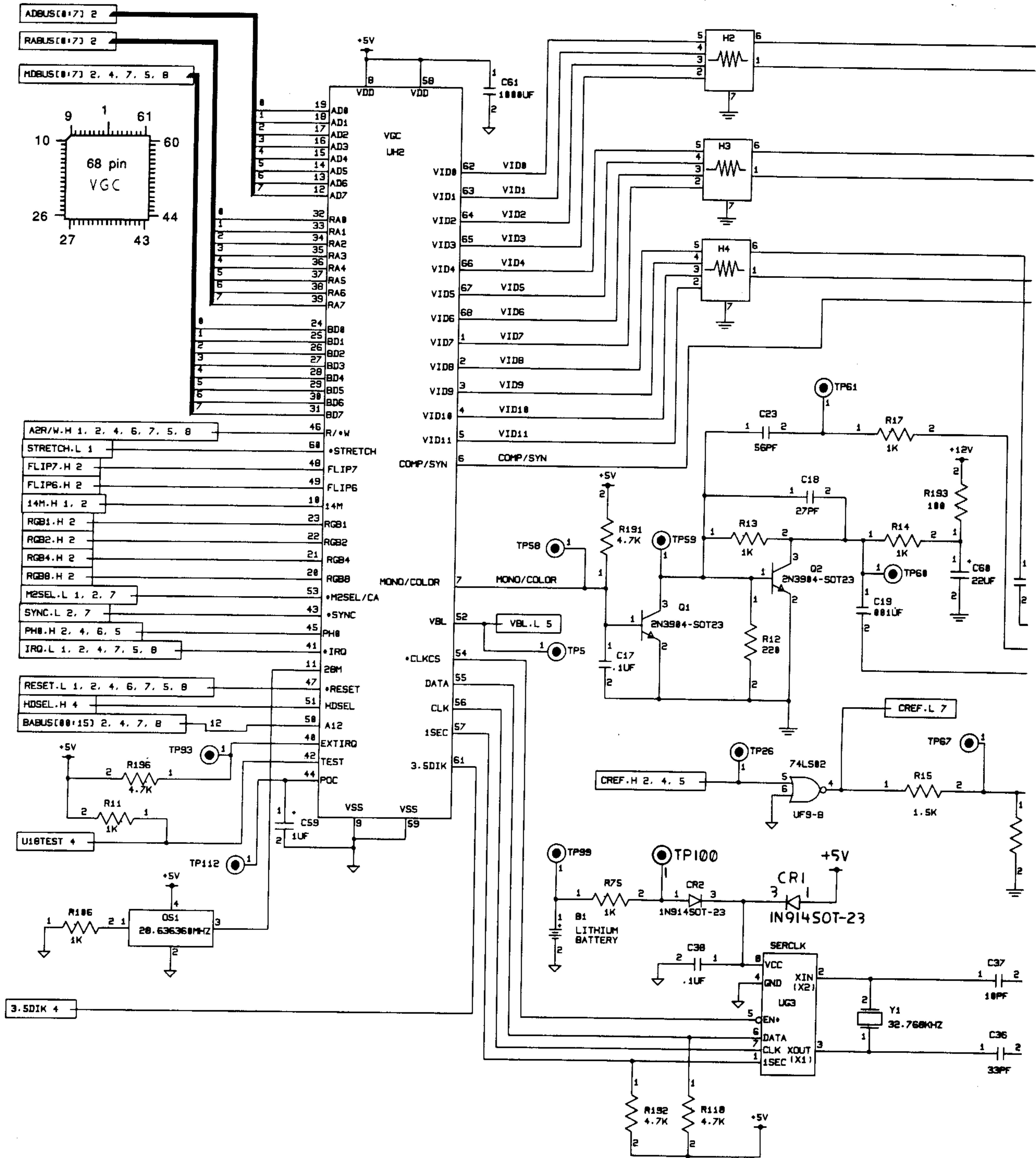
ADBUS[0:7]

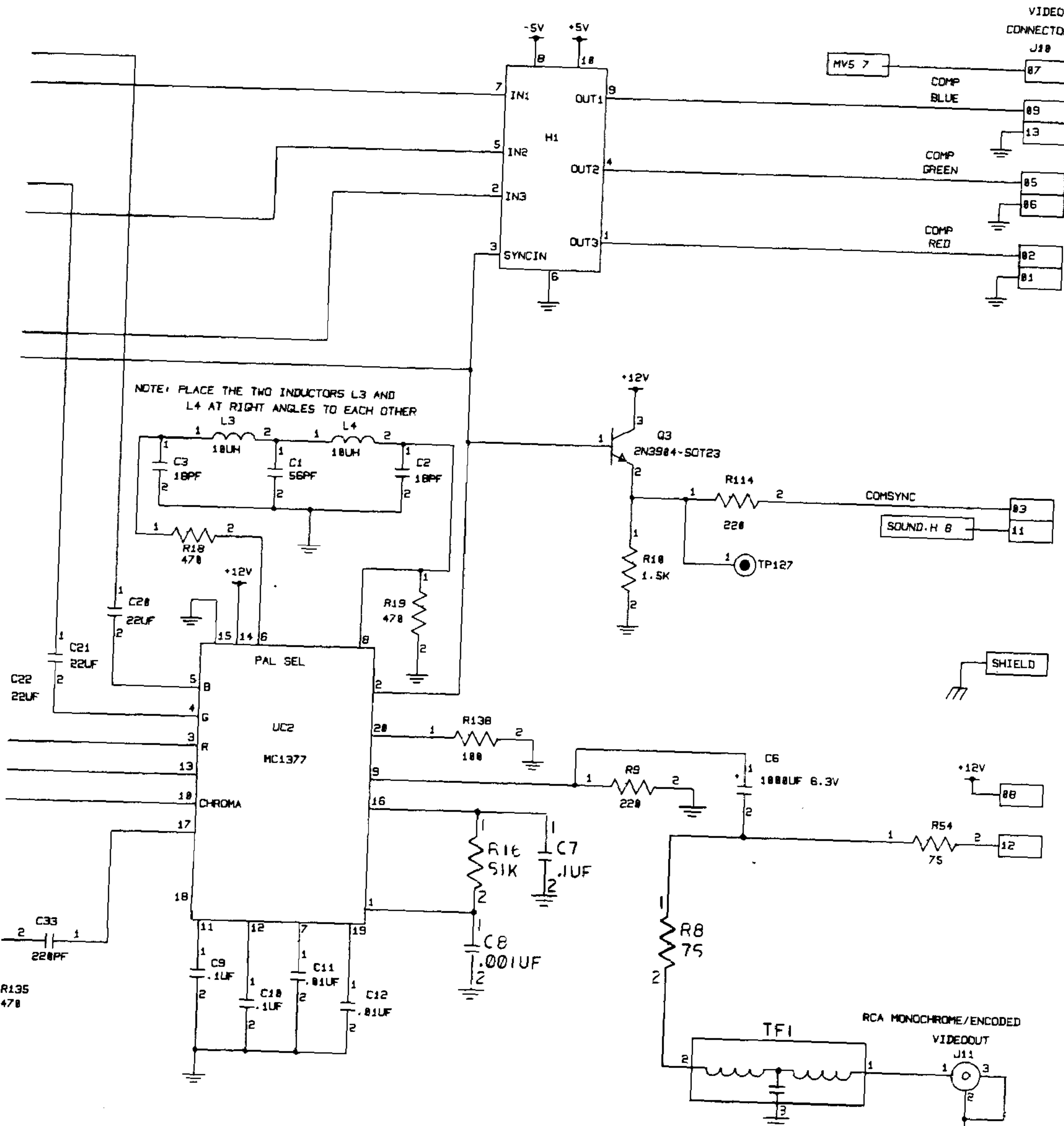
ADBUS[0:7]

SBUS[0:15]

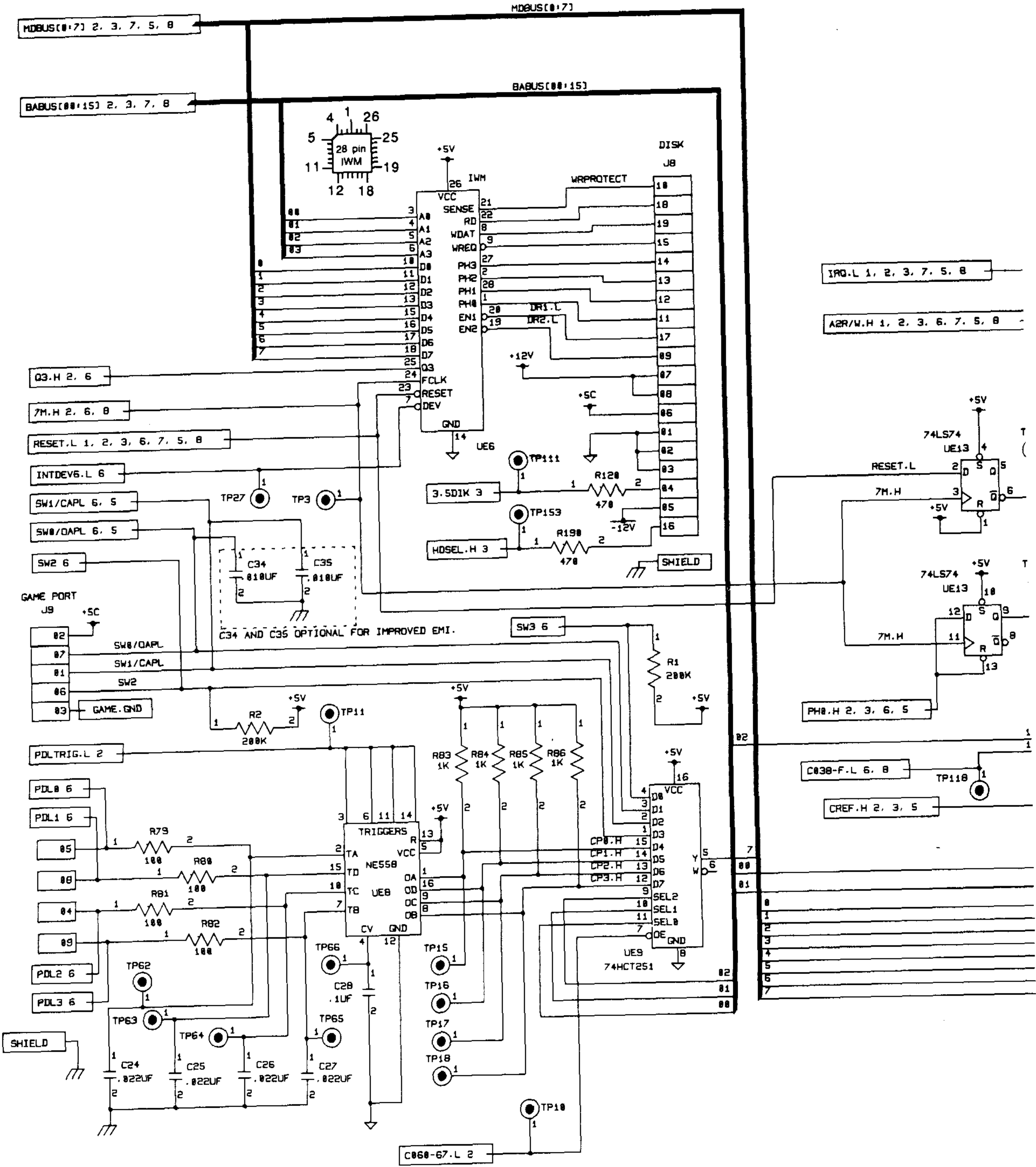
SBUS[0:15]

# Schematic diagram, Part 3

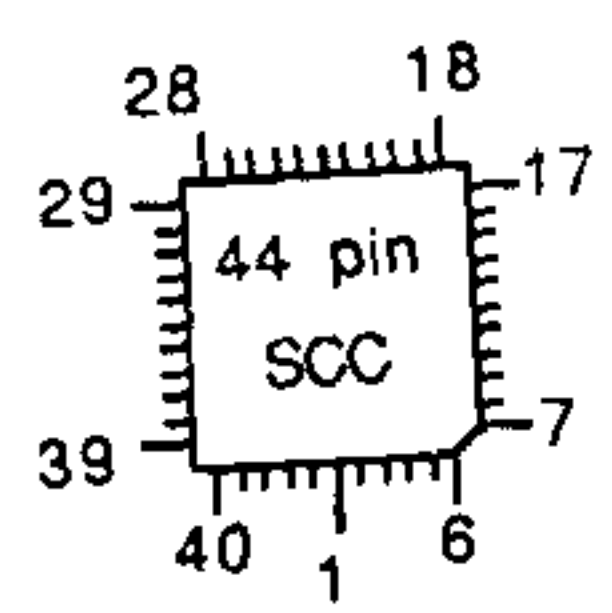
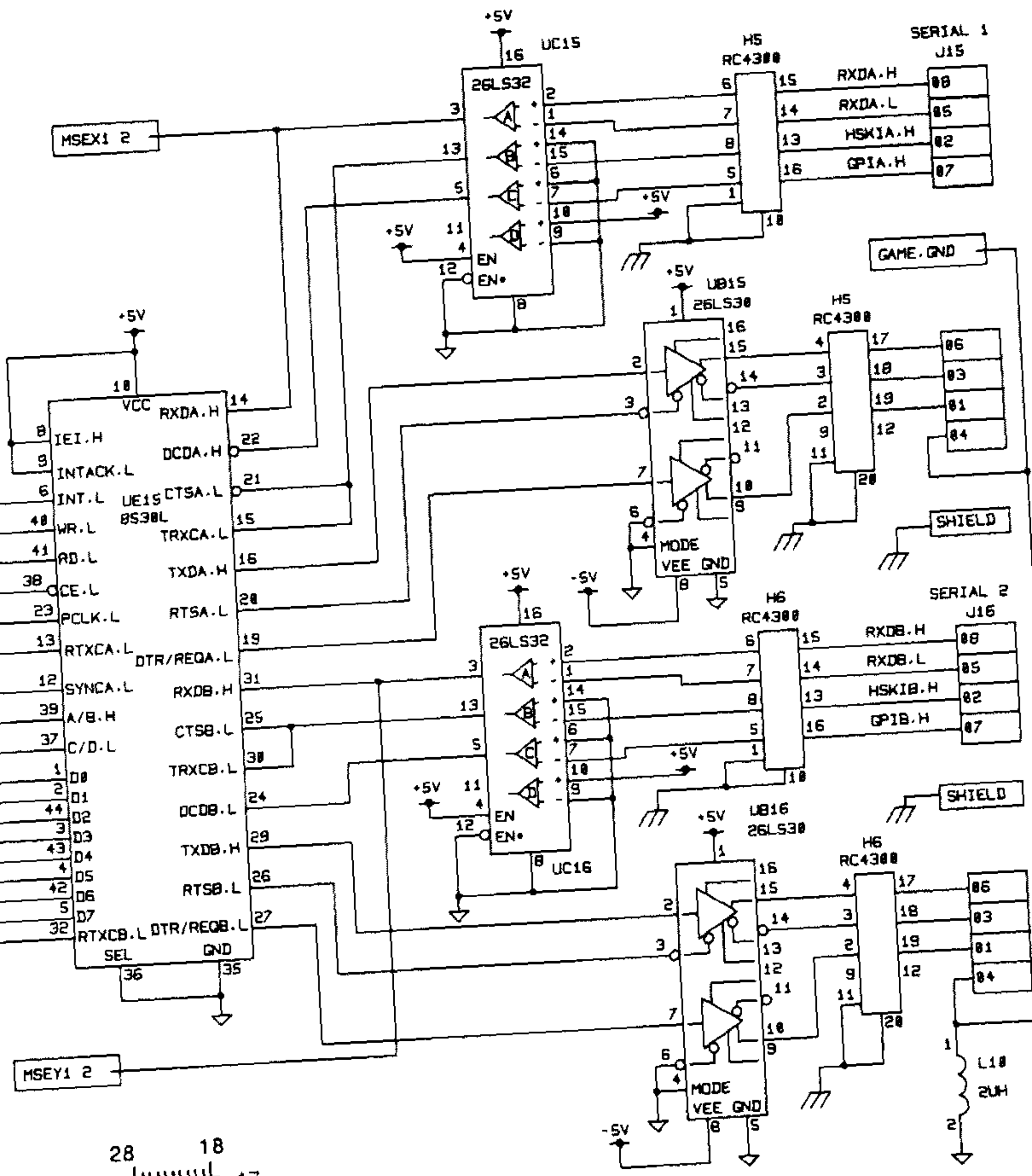
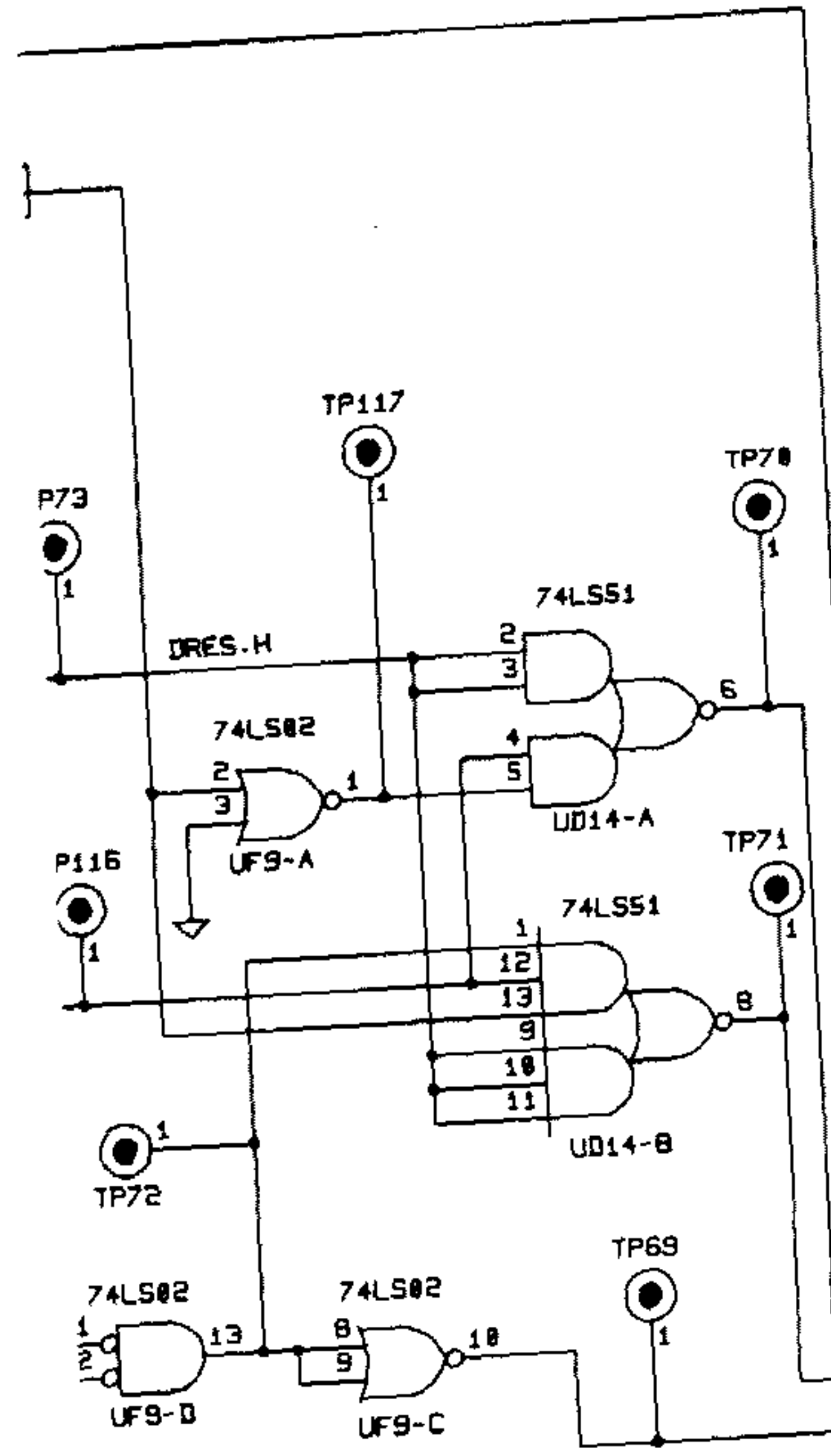
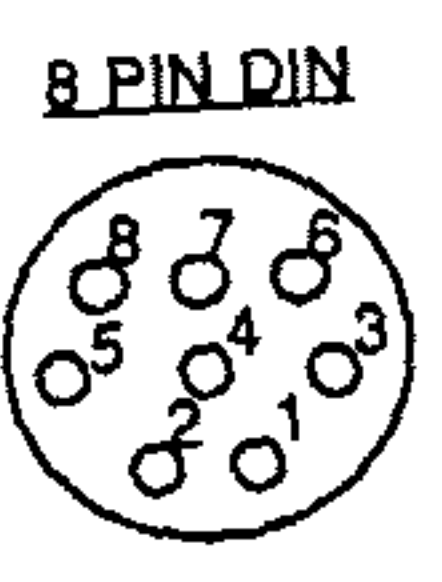
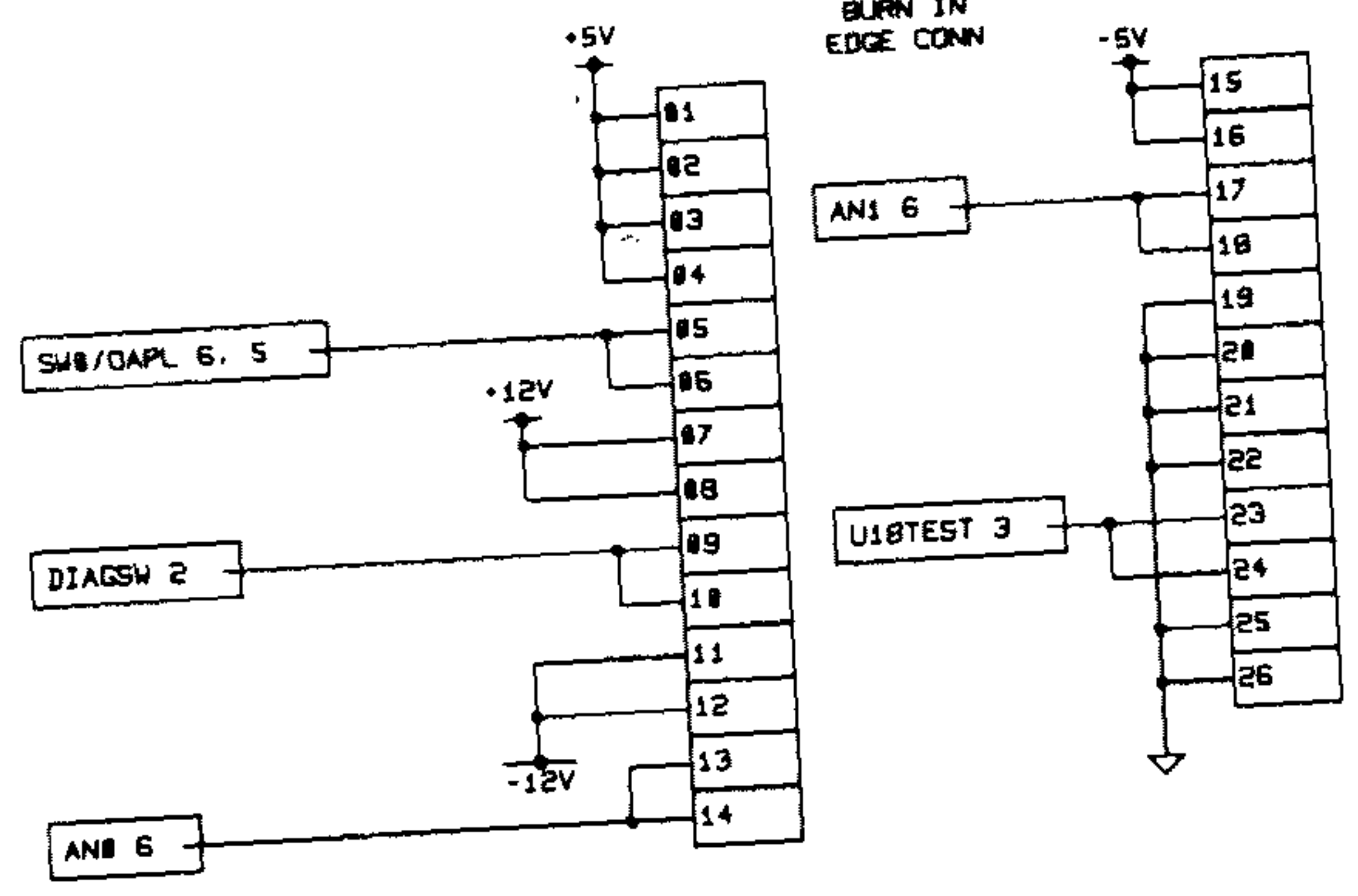




# Schematic diagram, Part 4

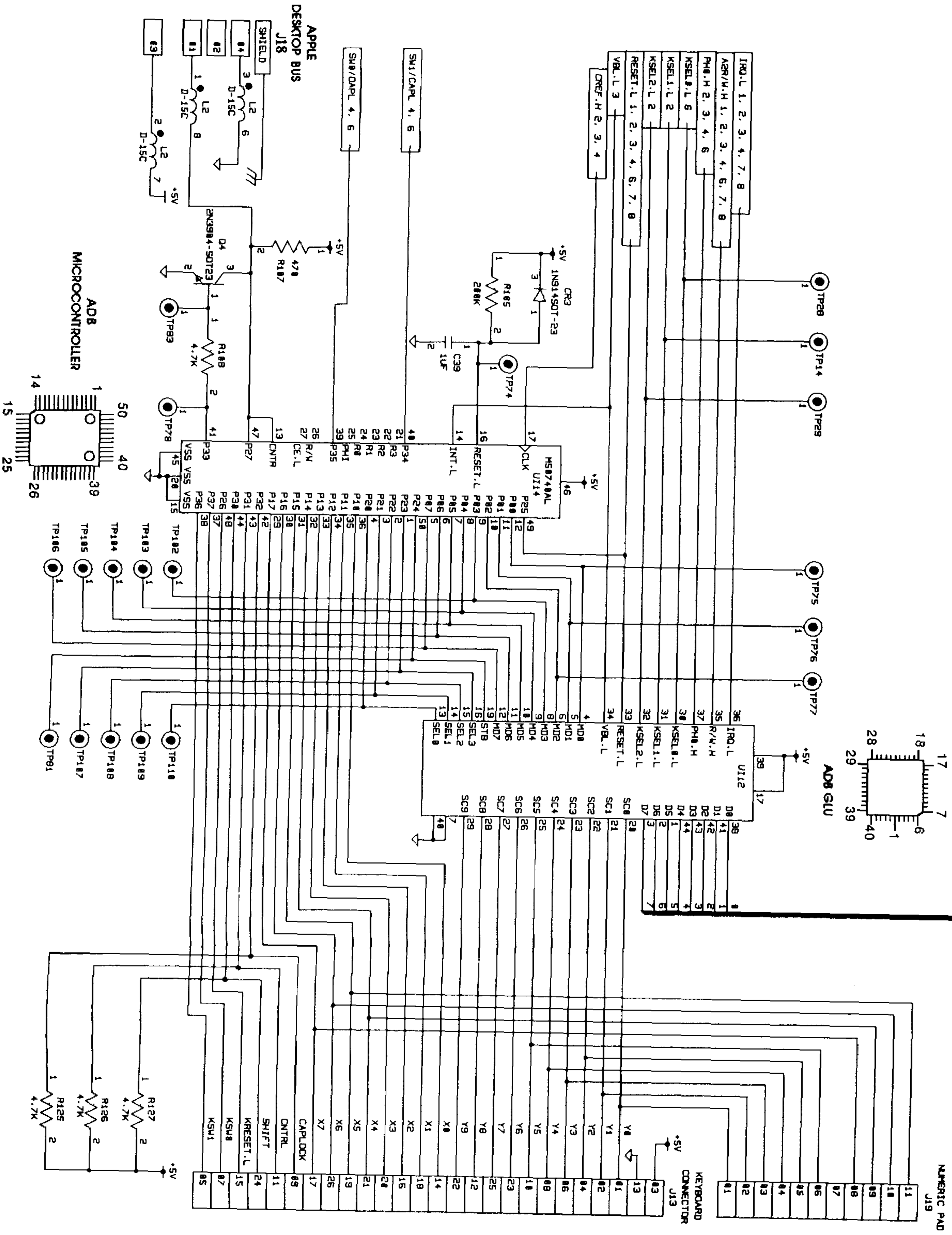


J23  
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EDGE CONN



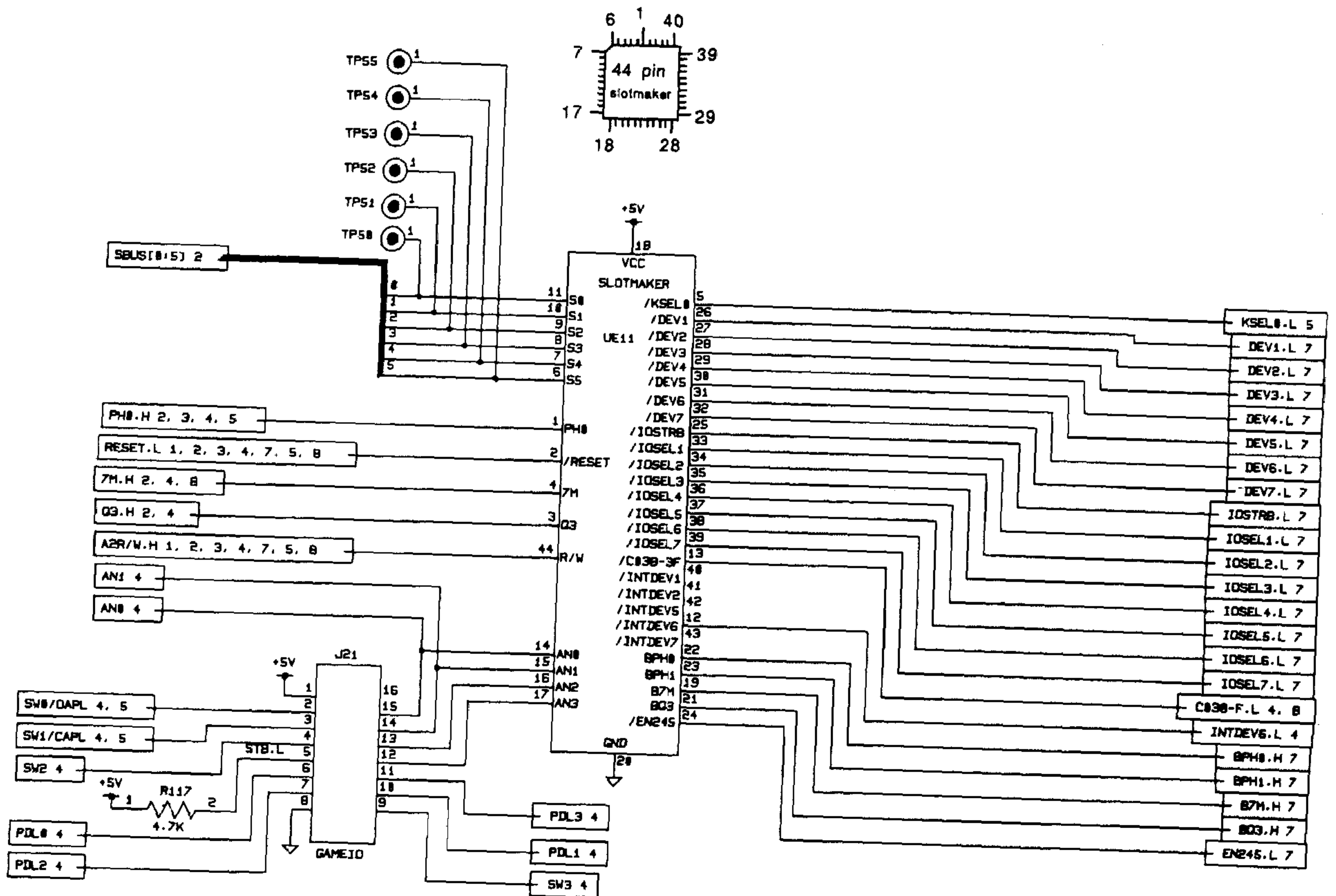
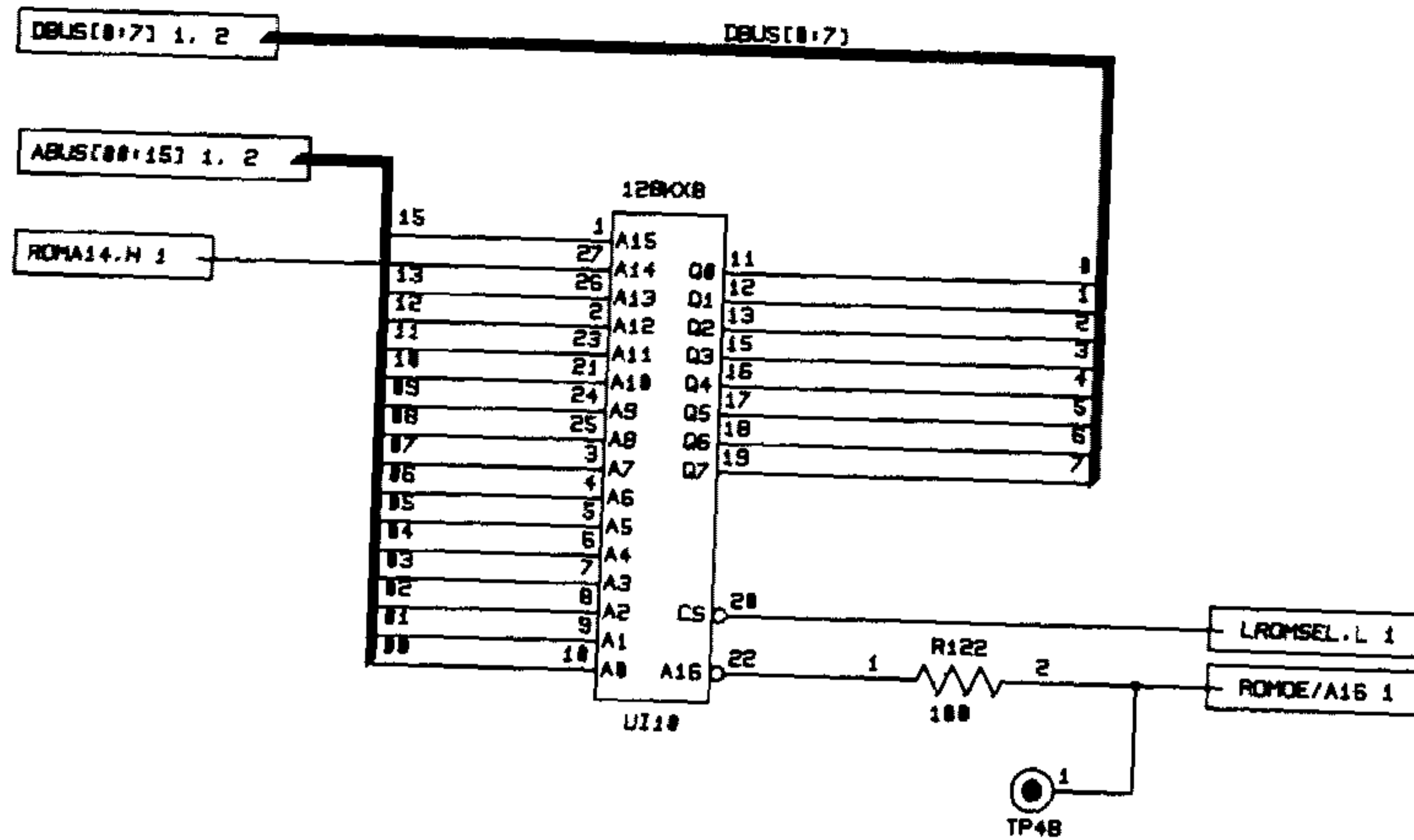
MOBUS(C17) 2, 3, 4, 7, 8

MOBUS(C17)

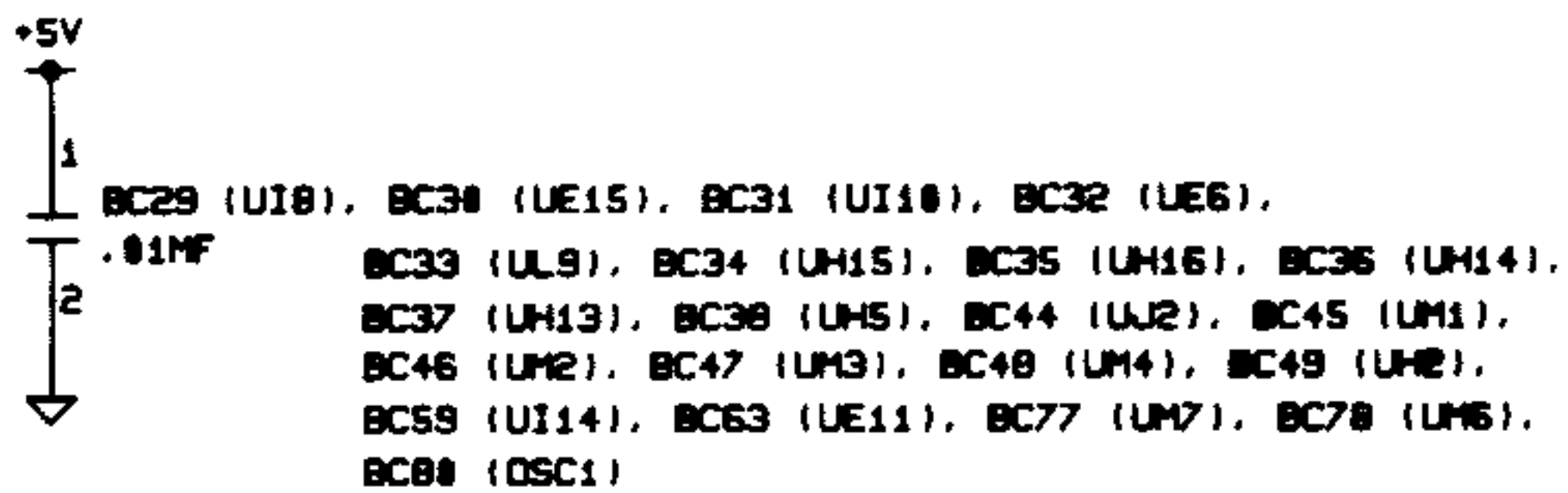
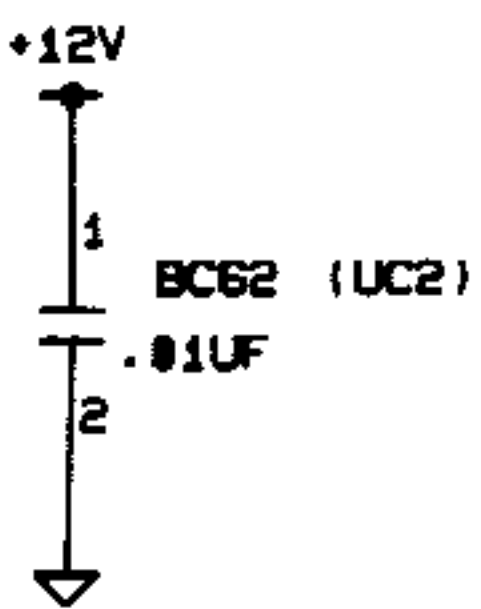
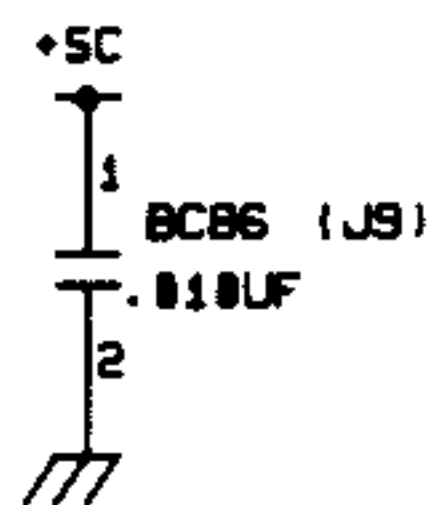
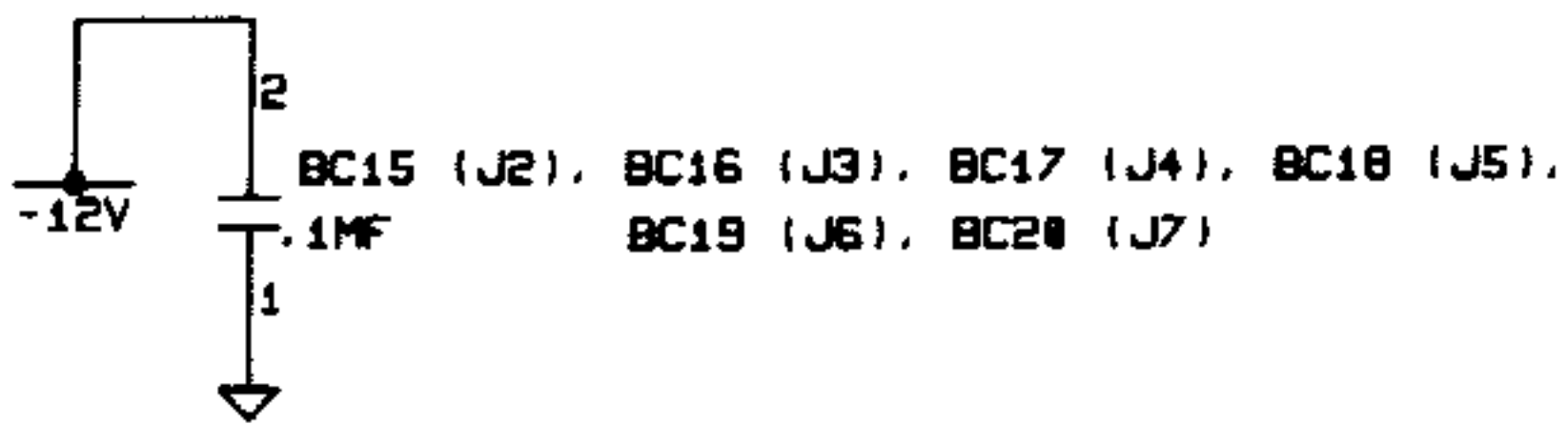
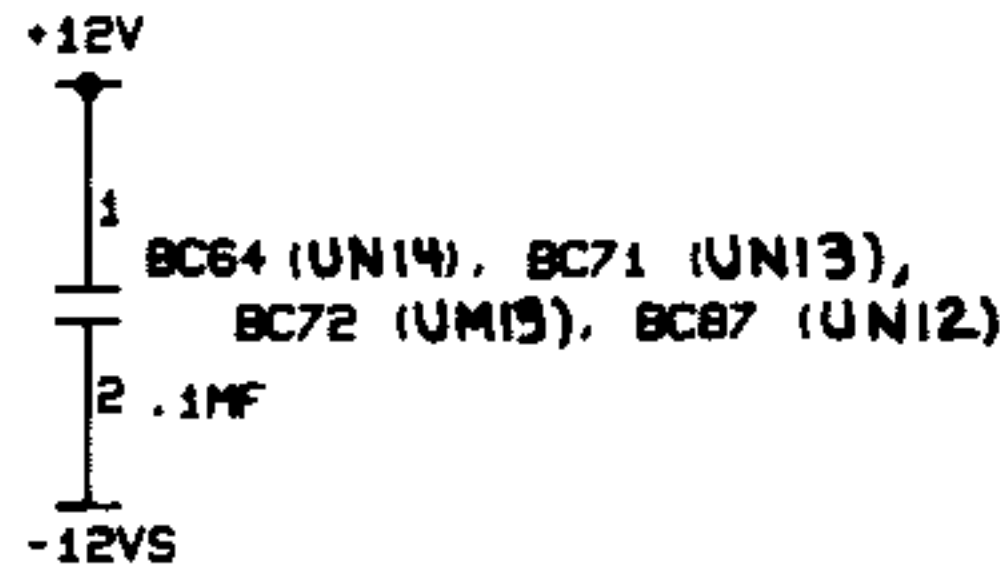
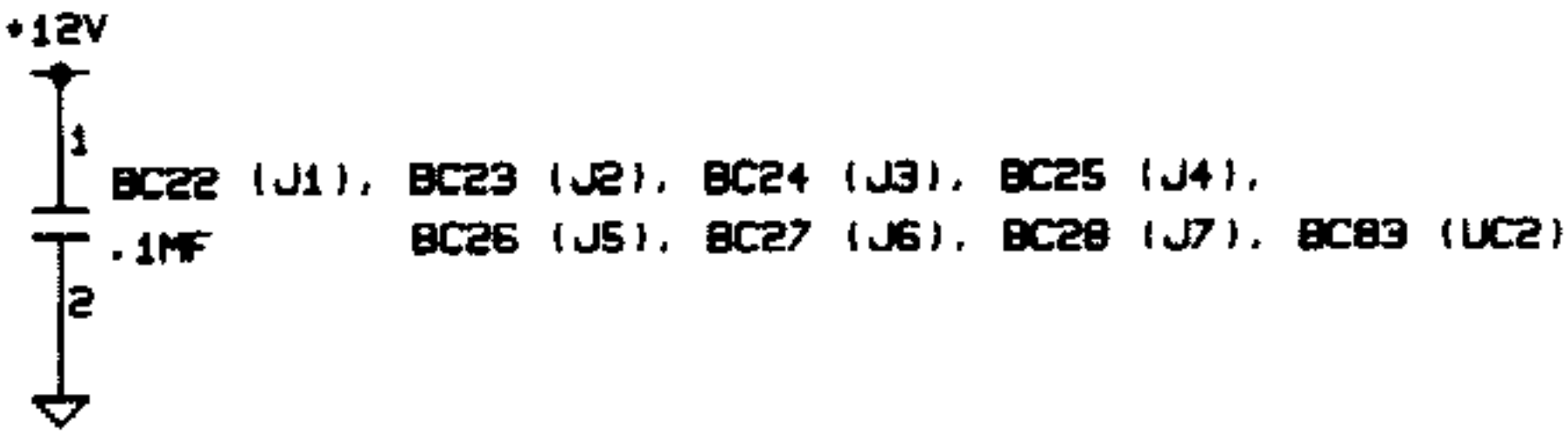
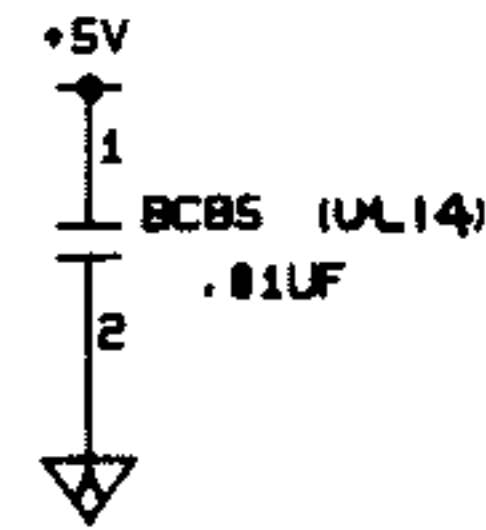
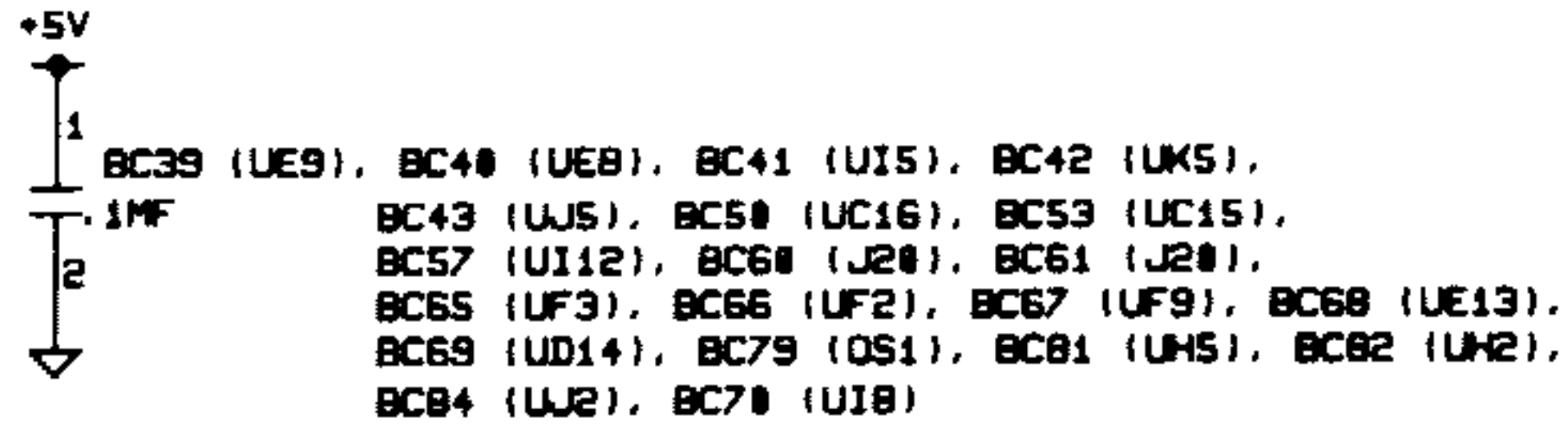
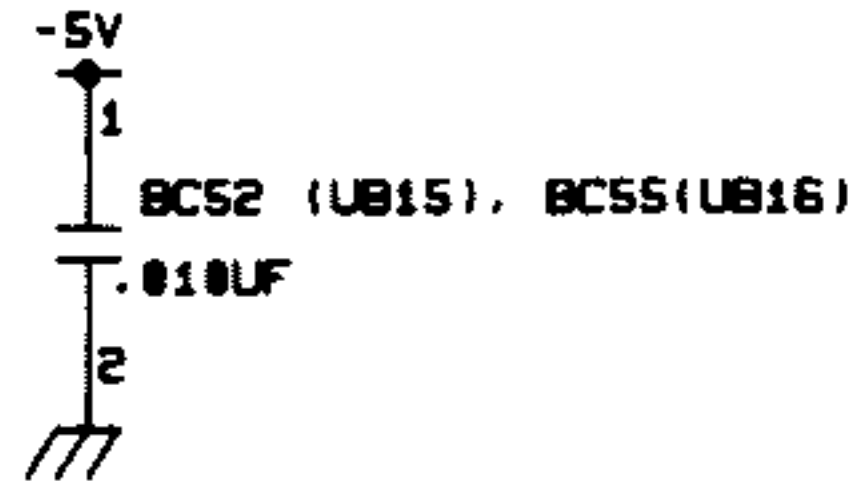
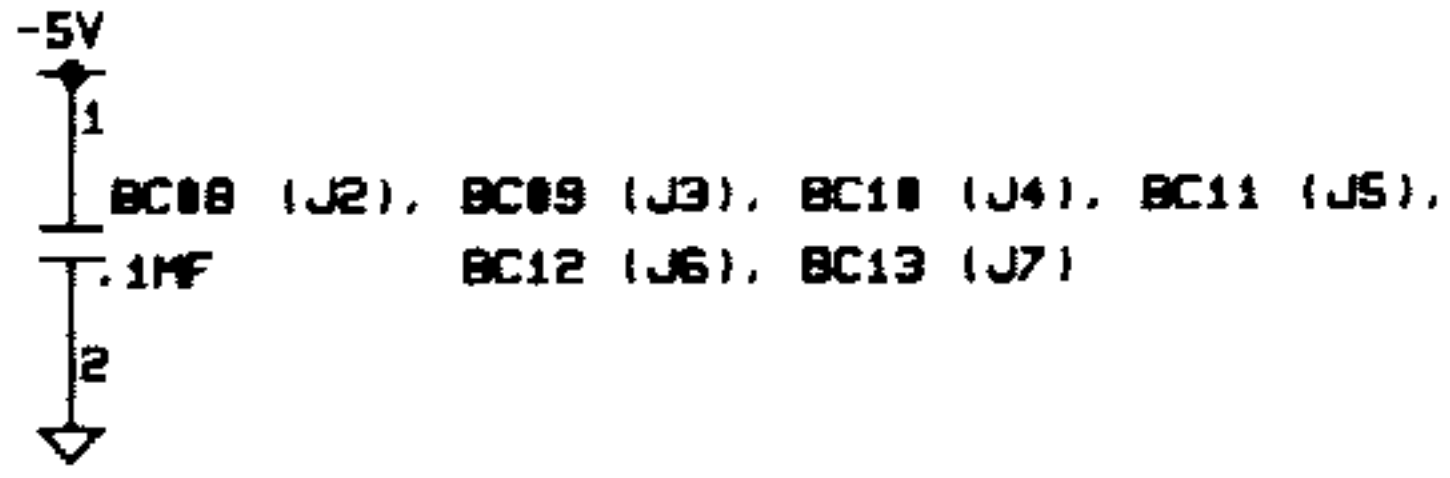
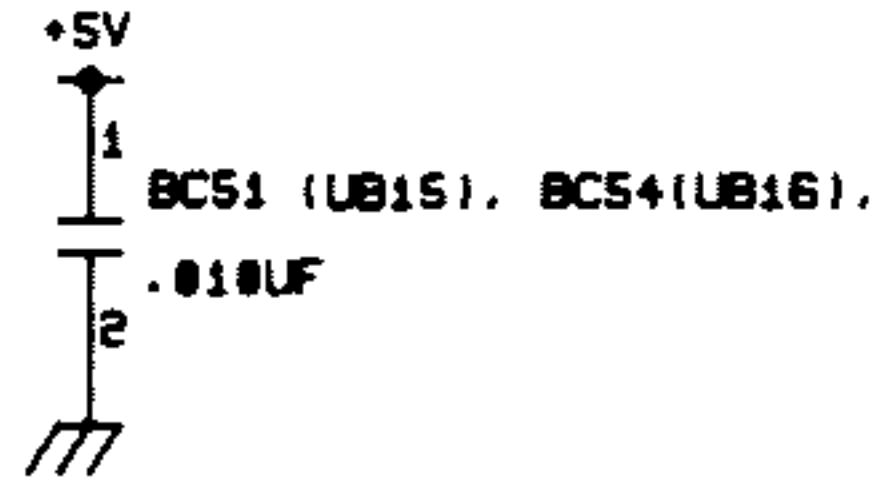
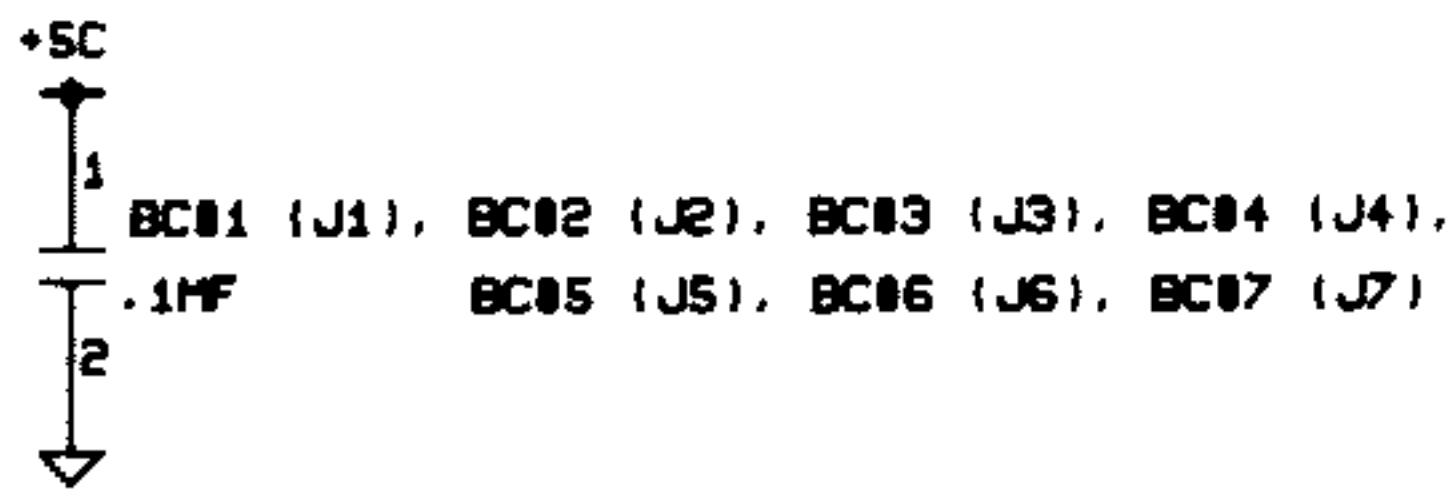




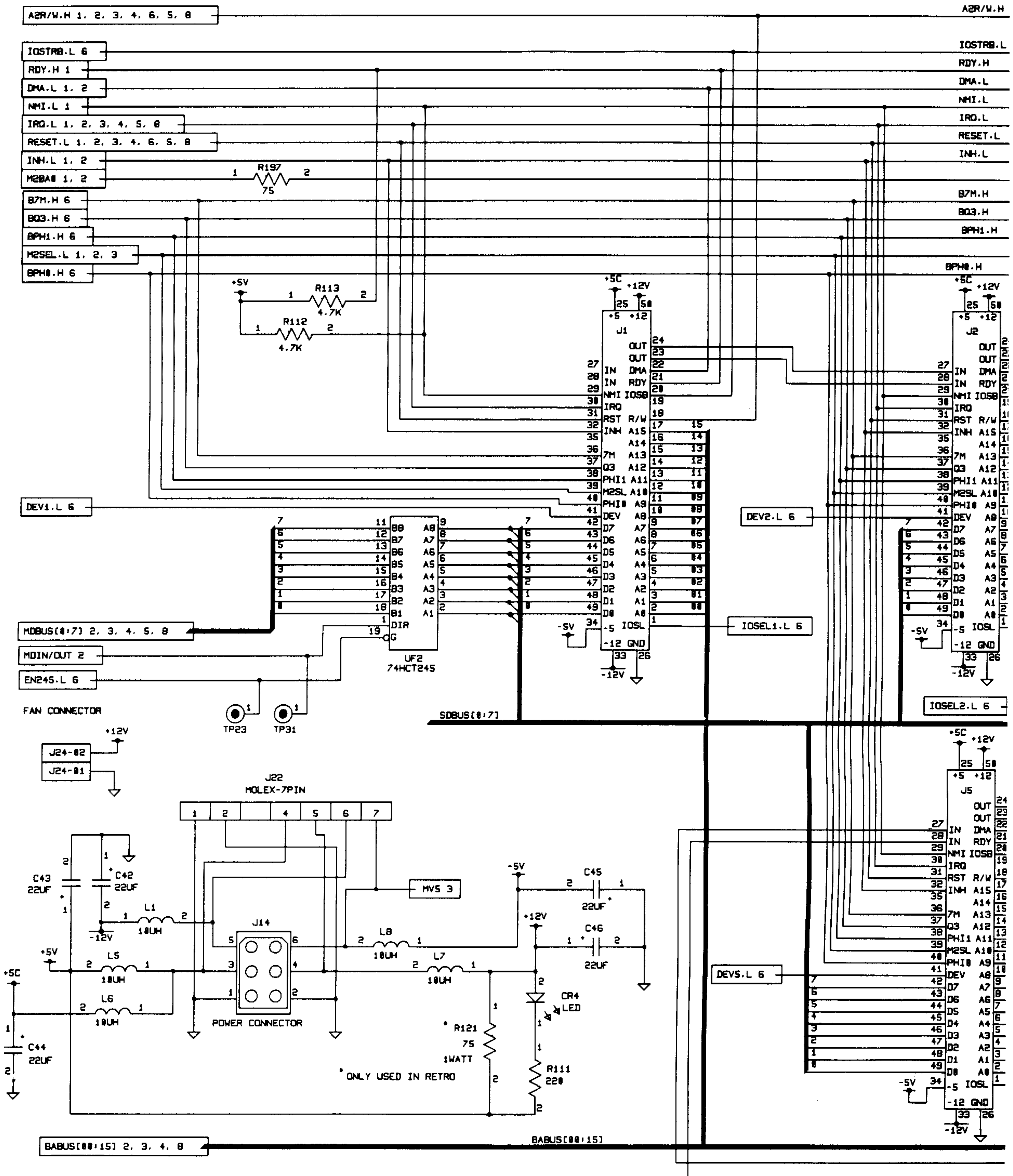
# Schematic diagram, Part 6

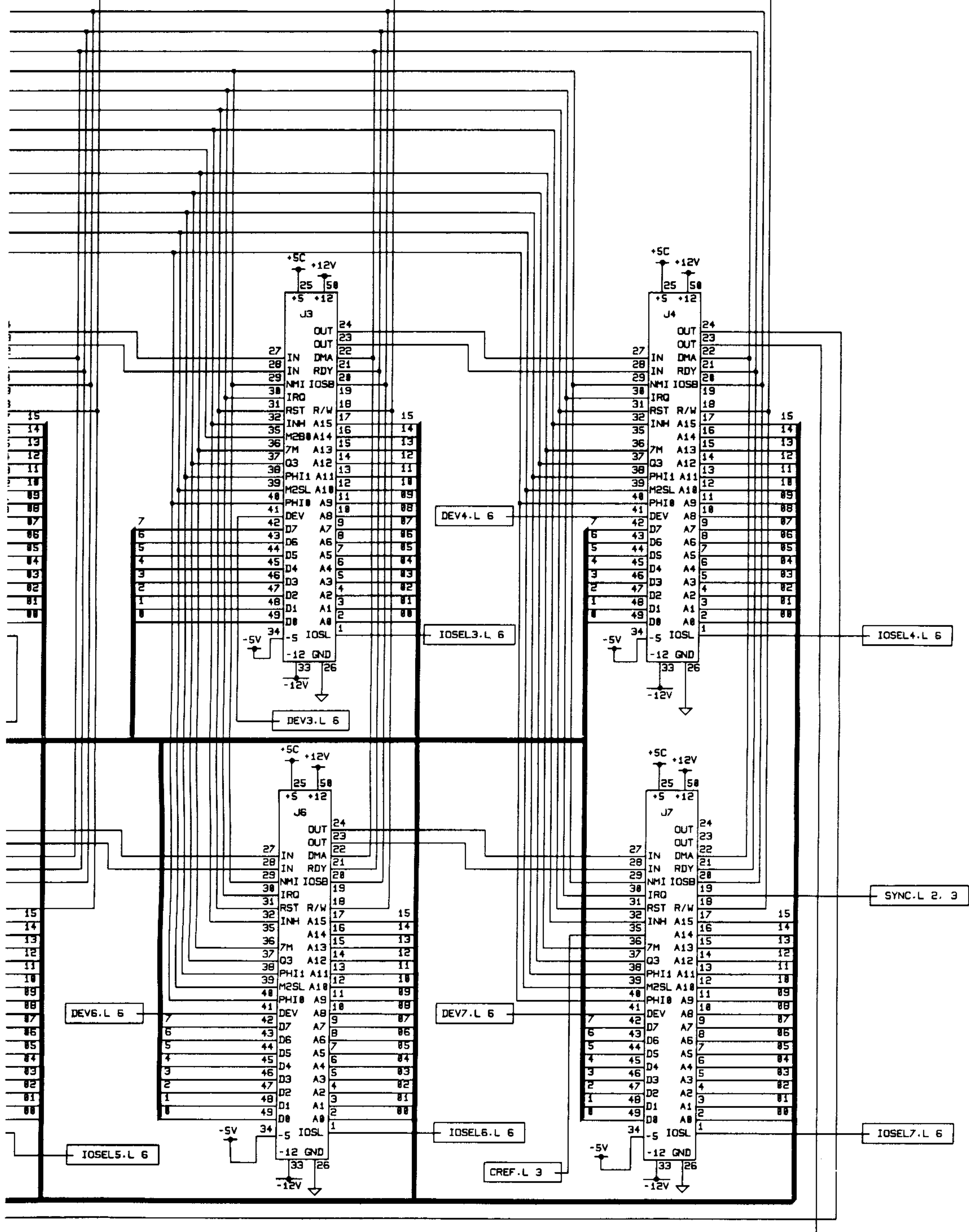


# BYPASS CAPACITORS



# Schematic diagram, Part 7

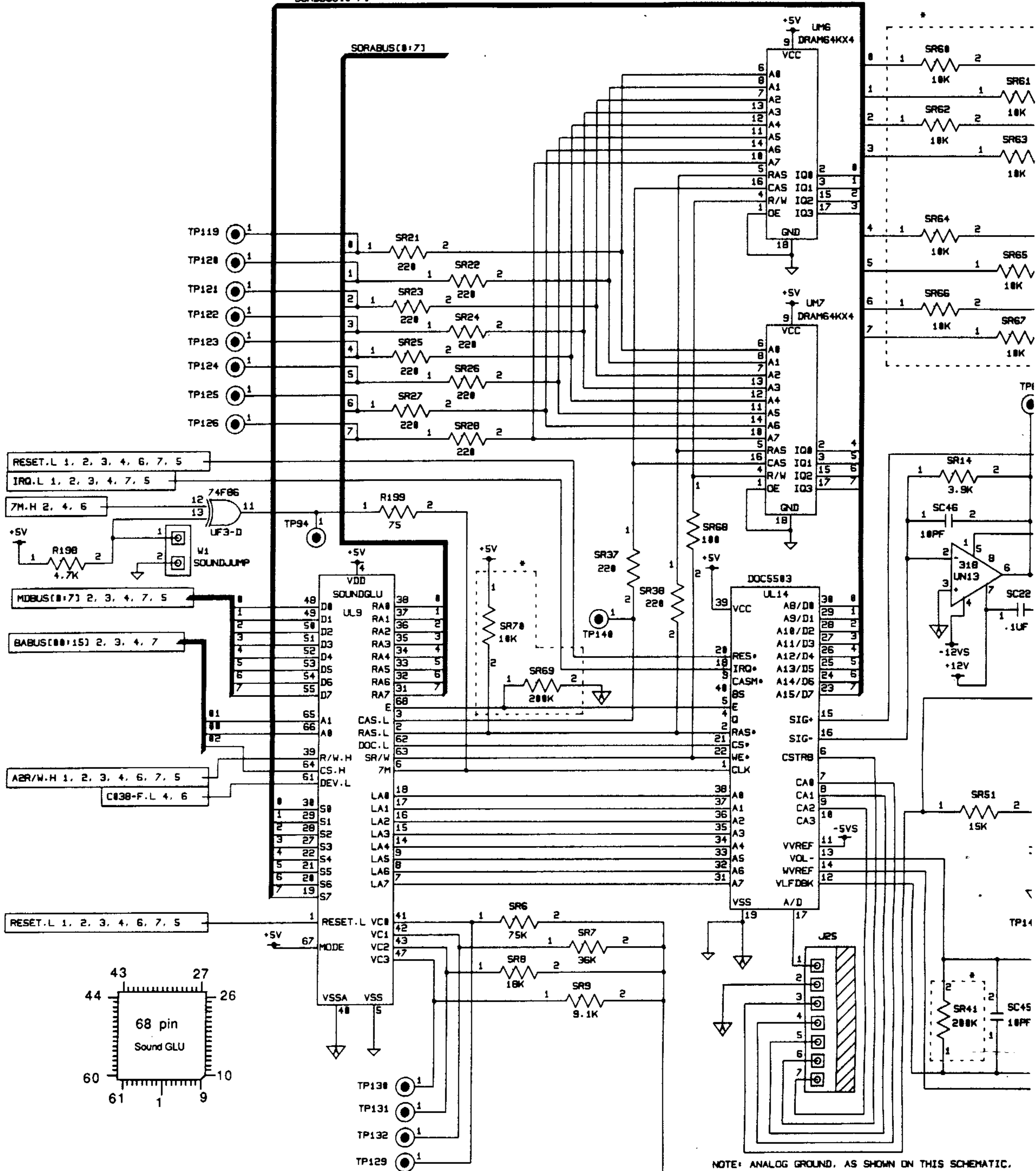




# Schematic diagram, Part 8

SOADBUS[0:7]

SORABUS[0:7]



NOTE: ANALOG GROUND, AS SHOWN ON THIS SCHEMATIC, SHALL BE SEPARATE FROM DIGITAL GROUND. DIGITAL GROUND WILL TIE INTO THE DOC-5503 (UL14) AT ONE POINT ONLY, PIN 19, AND THIS POINT WILL ALSO BE THE ONLY PLACE WHERE ANALOG GROUND TIES TO DIGITAL GROUND.

\* THESE RESISTORS ARE NOT NEEDED IF THE DOC5503 (UL14) IS ON THE BOARD.

